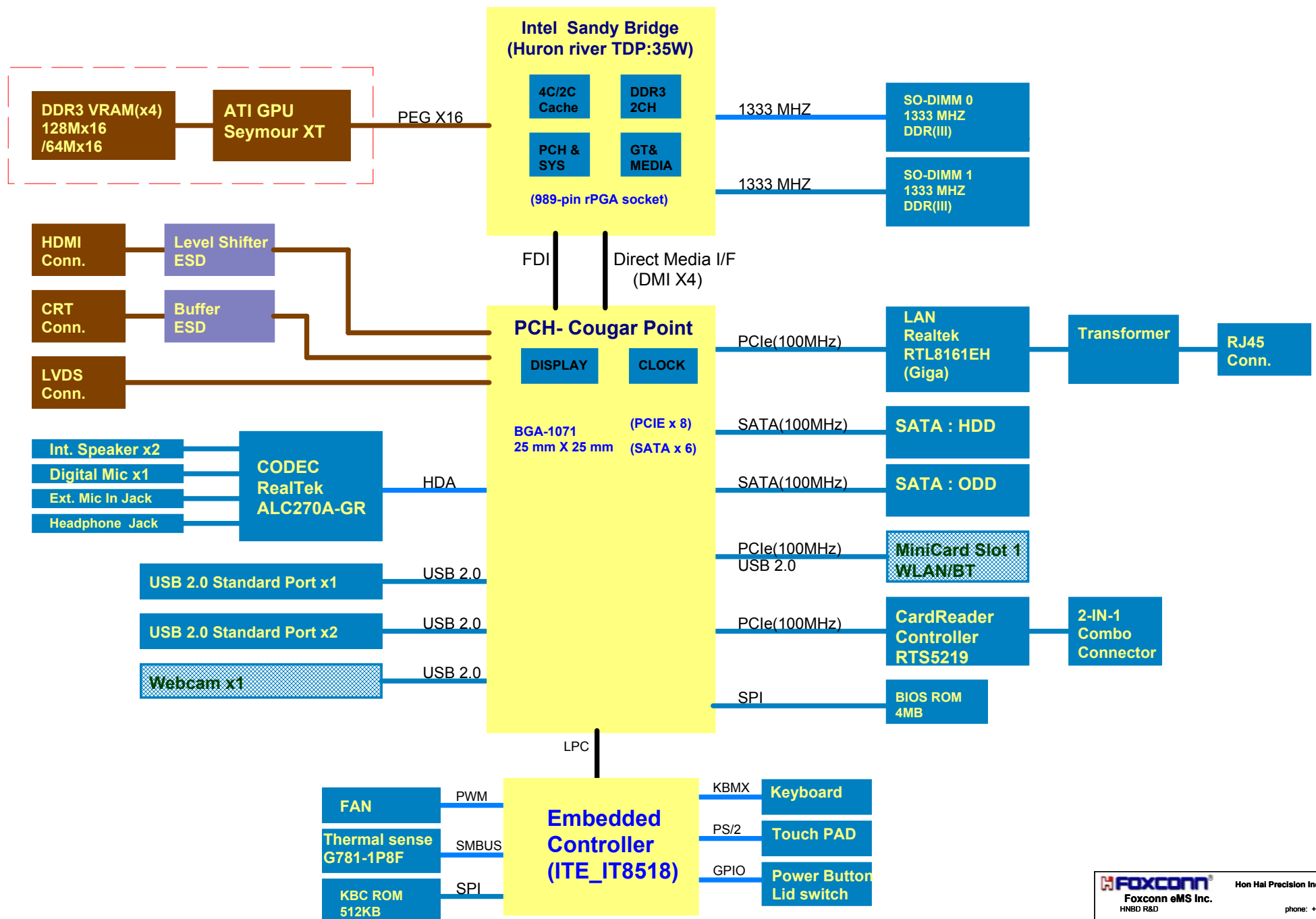


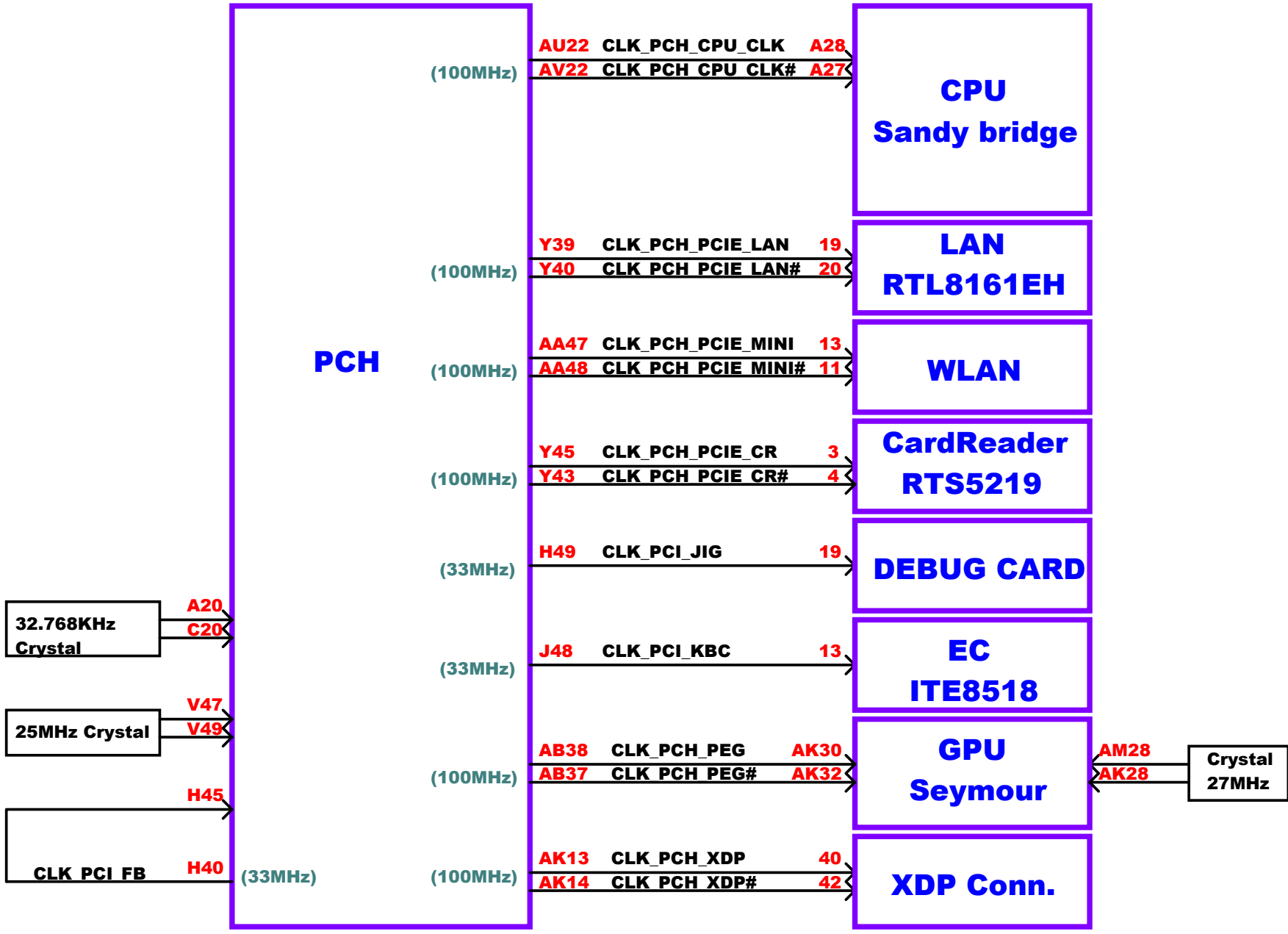
PROJECT : CHICAGO (For Intel Huron River Platform)

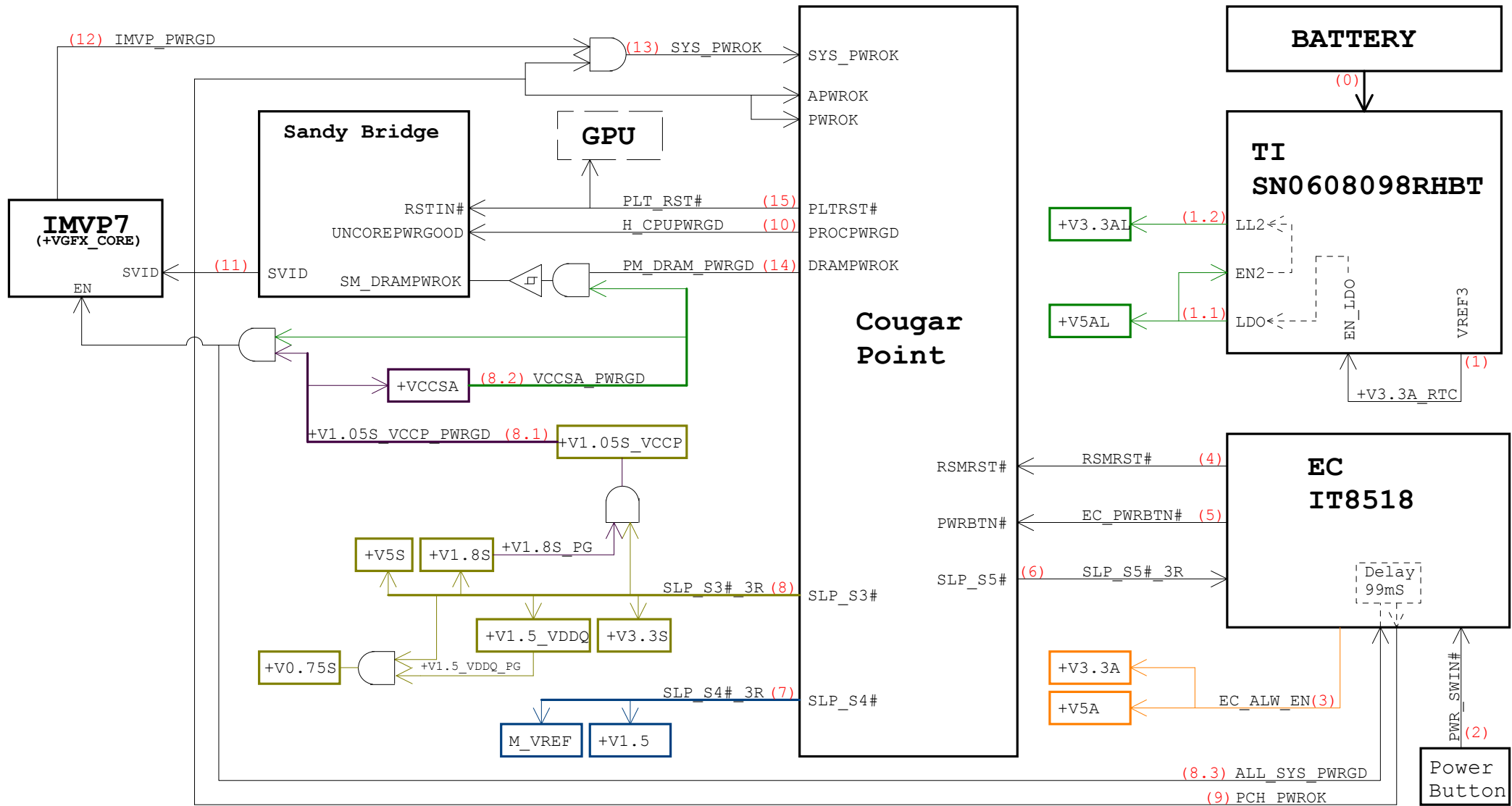
01 -- COVER SHEET	23 -- CougarPoint (HDA, SATA..)
02 -- SYSTEM BLOCK DIAGRAM	24 -- CougarPoint (PCI-E, CLK..)
03 -- CLOCK MAP	25 -- CougarPoint (DMI, FDI..)
04 -- POWER SEQUENCY DIAGRAM	26 -- CougarPoint (USB, GPIO..)
05 -- POWER MAP	27 -- CougarPoint (PWR/GND)
06 -- SMBUS MAP	28 -- CougarPoint (PWR, GND)
07 -- Blank	29 -- DDR3 (SO-DIMM 0&1)
08 -- DCIN/BATT	30 -- VGA (PCI-E/STRAP) 1/3
09 -- PWR_CHARGE	31 -- VGA_S3 (IO) 2/3
10 -- PWR_5V/3.3V	32 -- VGA_S3 (DDR3) 3/3
11 -- PWR_VCCP	33 -- VRAM (DDR3)
12 -- PWR_1.5V/0.75S	34 -- EC+KBC (IT8518) & ROM
13 -- PWR_VCORE	35 -- Audio (CODEC_ALC270A)
14 -- PWR_OTHER	36 -- Audio (JACK+AMP+SPK+Mute)
15 -- PWR_ATVDD	37 -- LAN (RTL8161EH)
16 -- PWR_1.8VS	38 -- Mini PCIe & FAN
17 -- PWR_VCCSA	39 -- USBx2/USB DB/SATA CONN.
18 -- Sandy Bridge (DMI, PEG, FDI)	40 -- Card Reader (RTL5219-GR)
19 -- Sandy Bridge (CLK, JTAG..)	41 -- HDMI & CRT
20 -- Sandy Bridge (DDR3)	42 -- LVDS & Webcam
21 -- Sandy Bridge (PWR/GND)	43 -- Sequence circuit
22 -- Sandy Bridge (GRAPHIC PWR)	

P. Leader	Check by	Design by

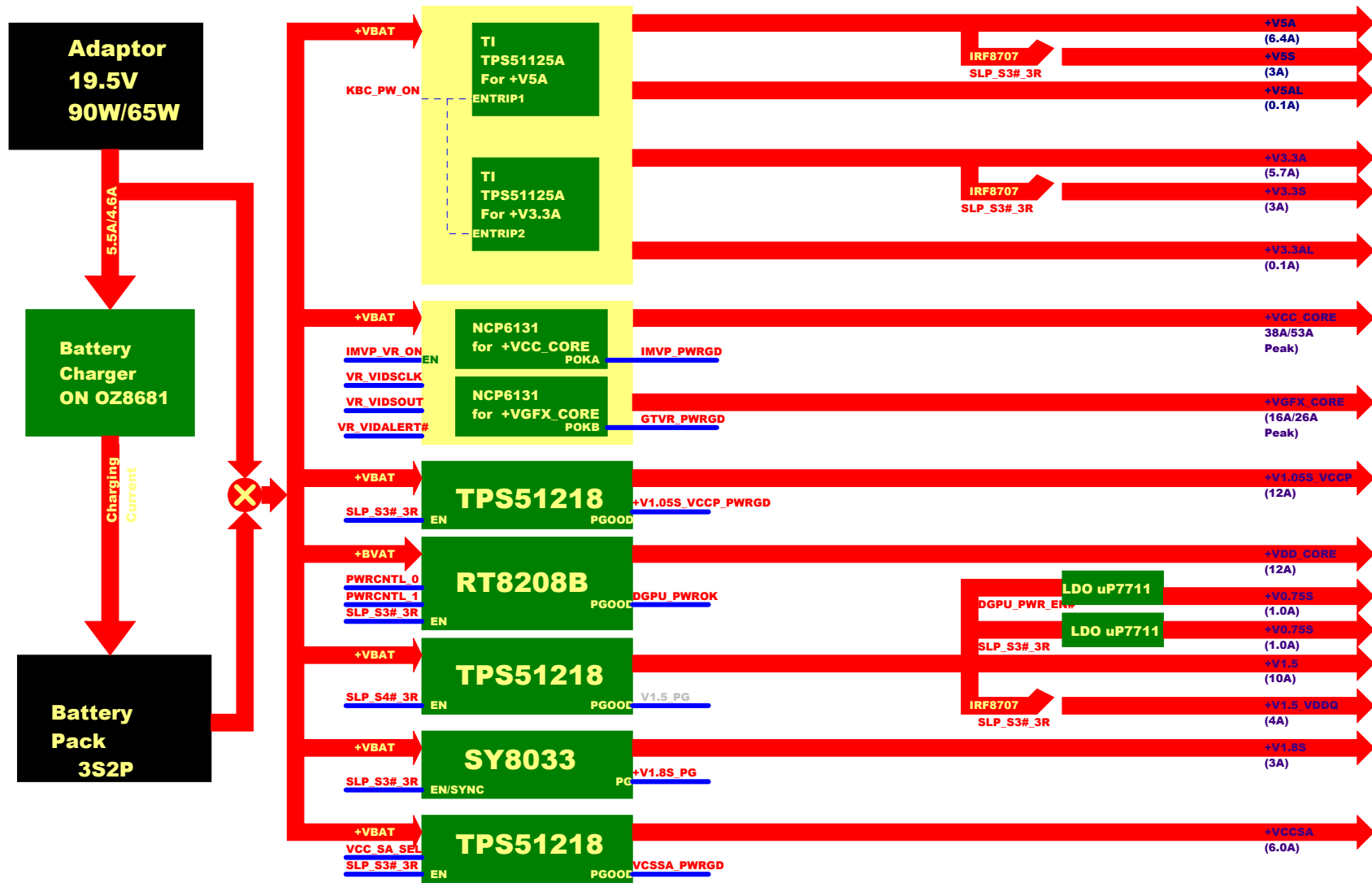
 Foxconn eMS Inc. HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111
Title		
Index Page		
Size	Document Number	Rev
Custom	CHICAGO	MV
Page Modified: Tuesday, March 06, 2011		08:28:58 (UTC/GMT) Sheet 1 of 43

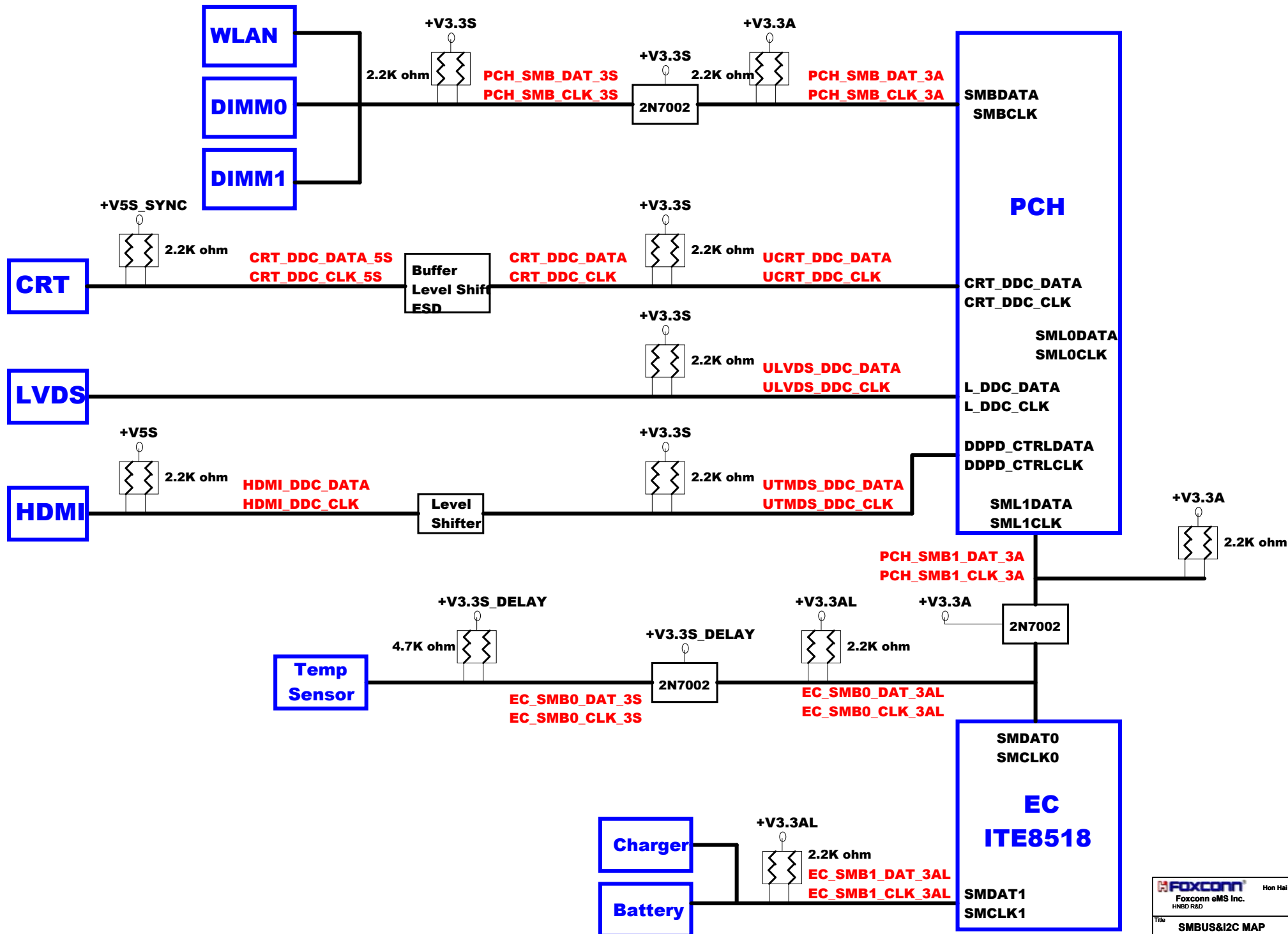






POWER MAP





D

C

B

A



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5

4

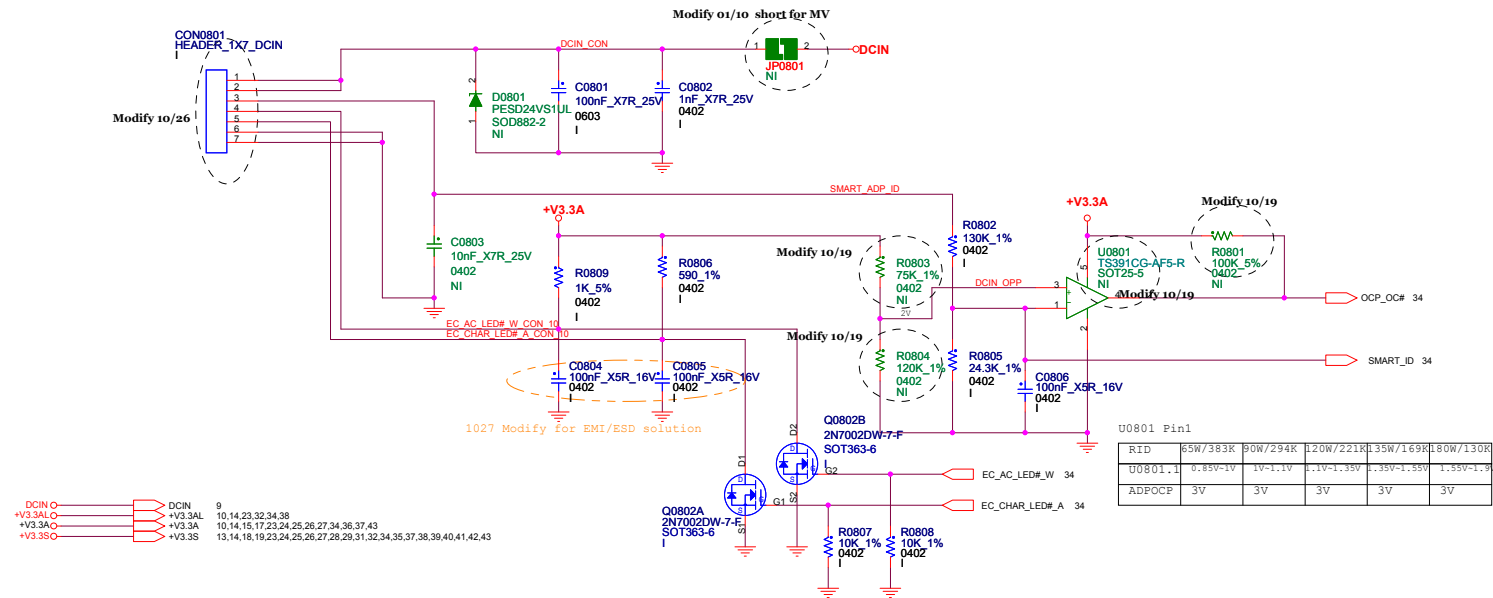
2

1

www.VinaFix.vn

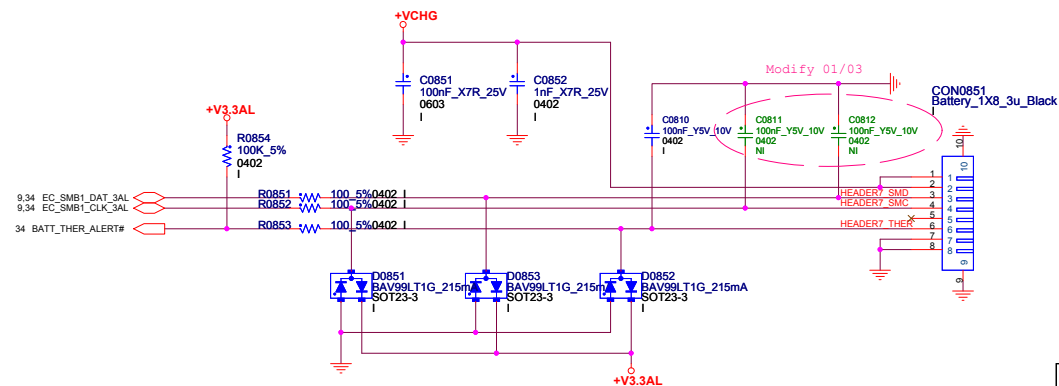
DC_JACK WIRE to BOARD CONNECTOR

2010.1203.0



BATTERY CONNECTOR

2010.0914.0

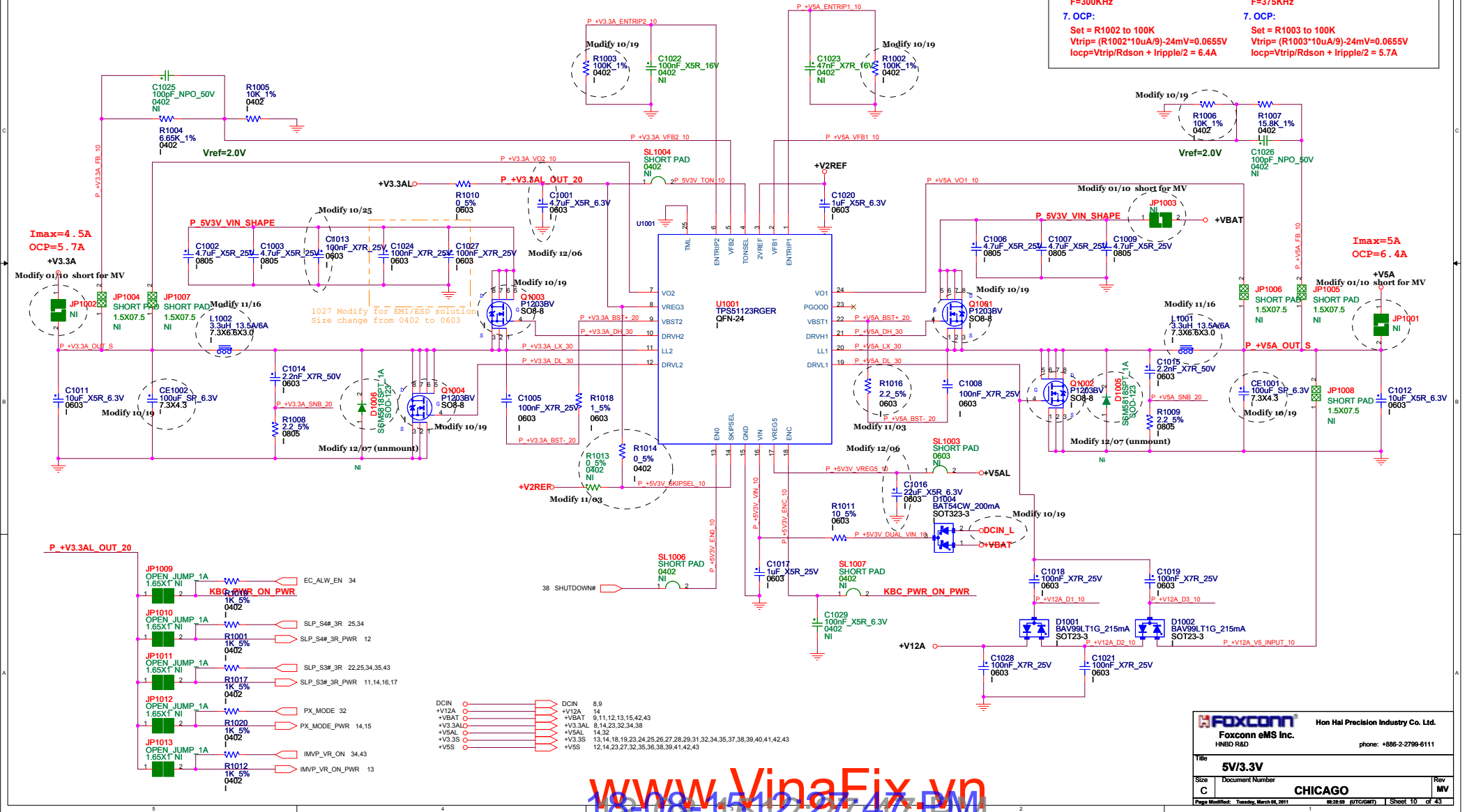


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18-08-1512:27:47 PM

+V5A / +V3.3A POWER SUPPLY

2010.1103.0

+V5A: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 3.7A$ 2. Ripple Current: $I_{rip} = 3.72A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 55.8mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: H-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 11A$ ($T = 25^\circ C$) $I_{peak} = 88A$ (Pause = 10 us) 6. Frequency: $F = 300KHz$ 7. OCP: $Set = R1002 \text{ to } 100K$ $V_{trip} = (R1002 \cdot 10uA/9) \cdot 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 6.4A$	+V3.3A: 1. I/P Current: $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.2A$ 2. Ripple Current: $I_{rip} = 2.21A$ 3. Ripple Voltage: $ESR/1 = 15mohm$ $V_{rip} = 33.15mV$ 4. Inductor Spec: $I_{sat} = 13.5A$ $I_{dc} = 6A$ $DCR = 30mohm$ 5. MOSFET Spec: L-side MOSFET: IRF8707PBF $R_{ds(ON)} = 17.5mohm$ ($V_{gs} = 4.5V$) $I_{cont} = 11A$ ($T = 25^\circ C$) $I_{peak} = 88A$ (Pause = 10 us) 6. Frequency: $F = 375KHz$ 7. OCP: $Set = R1003 \text{ to } 100K$ $V_{trip} = (R1003 \cdot 10uA/9) \cdot 24mV = 0.0655V$ $I_{ocp} = V_{trip} / R_{dson} + I_{ripple} / 2 = 5.7A$
---	--

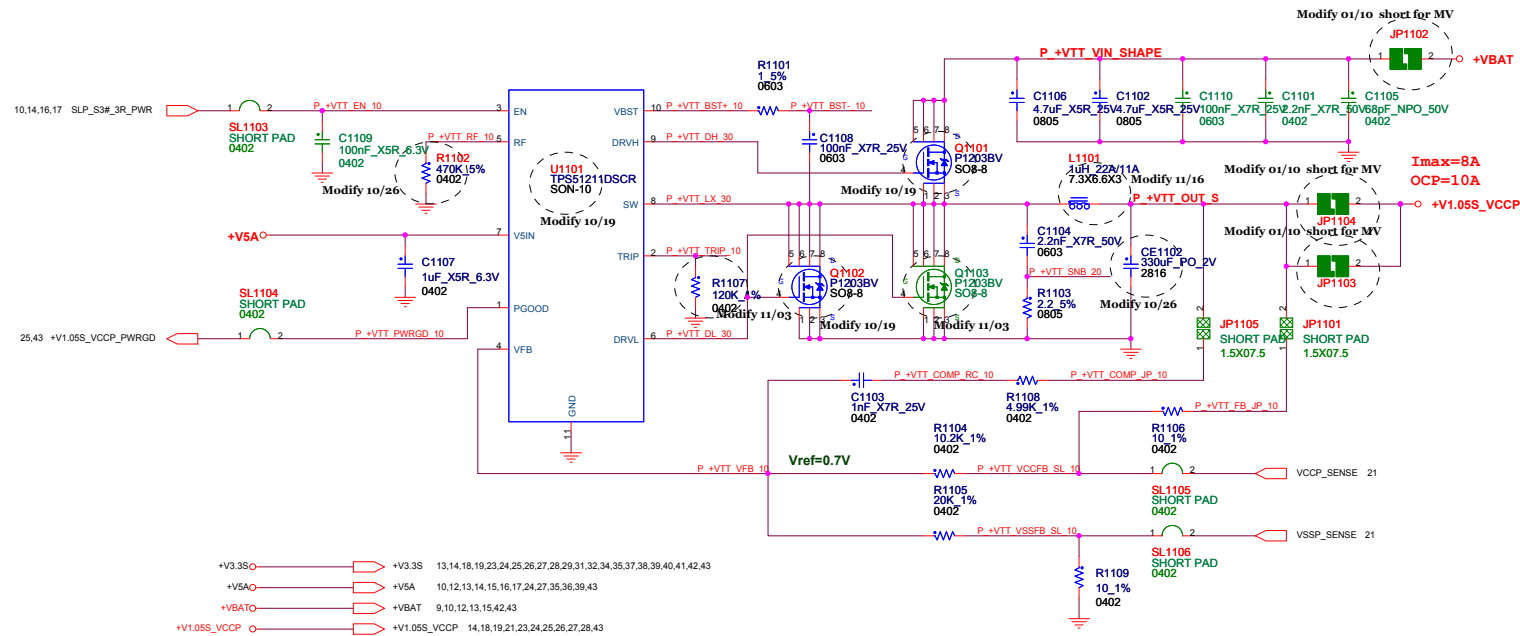


2010.1103.0

```

+V1.05S_VCCP:
1. I/P Current:
   Iin=Vo*Io/(0.75*Vin)=1.24A
2. Ripple Current:
   Irip=3.42A
3. Ripple Voltage:
   ESR/1=9mohm
   Vrip=30.78mV
4. Inductor Spec:
   Isat=36A
   Idc=18A
   DCR=3.3mohm
5. MOSFET Spec:
   H-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 °C)
   I peak = 88A (Pause =10 us)
   L-side MOSFET: IRF8707PBF
   Rds(ON)=17.5mohm (Vgs=4.5 V)
   I cont = 11A (T =25 °C)
   I peak = 88A (Pause =10 us)
6. Frequency:
   F=290KHz (R1102=0ohm)
7. OCP:
   Set = R1107 to 120K
   Vtrip= R1107*10uA=1.2V
   Iocp=(Vtrip/8*Rdson) + Iripple/2 = 10A

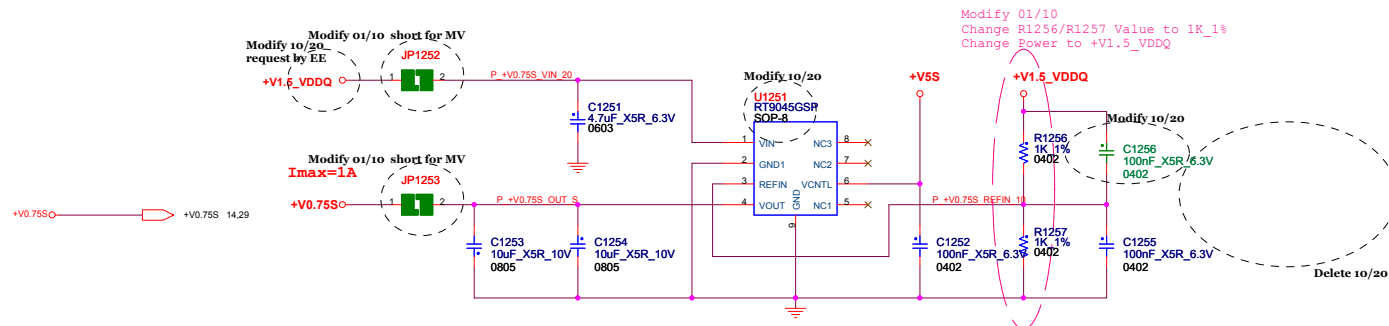
```



2010.1026.0



2010.1026.0

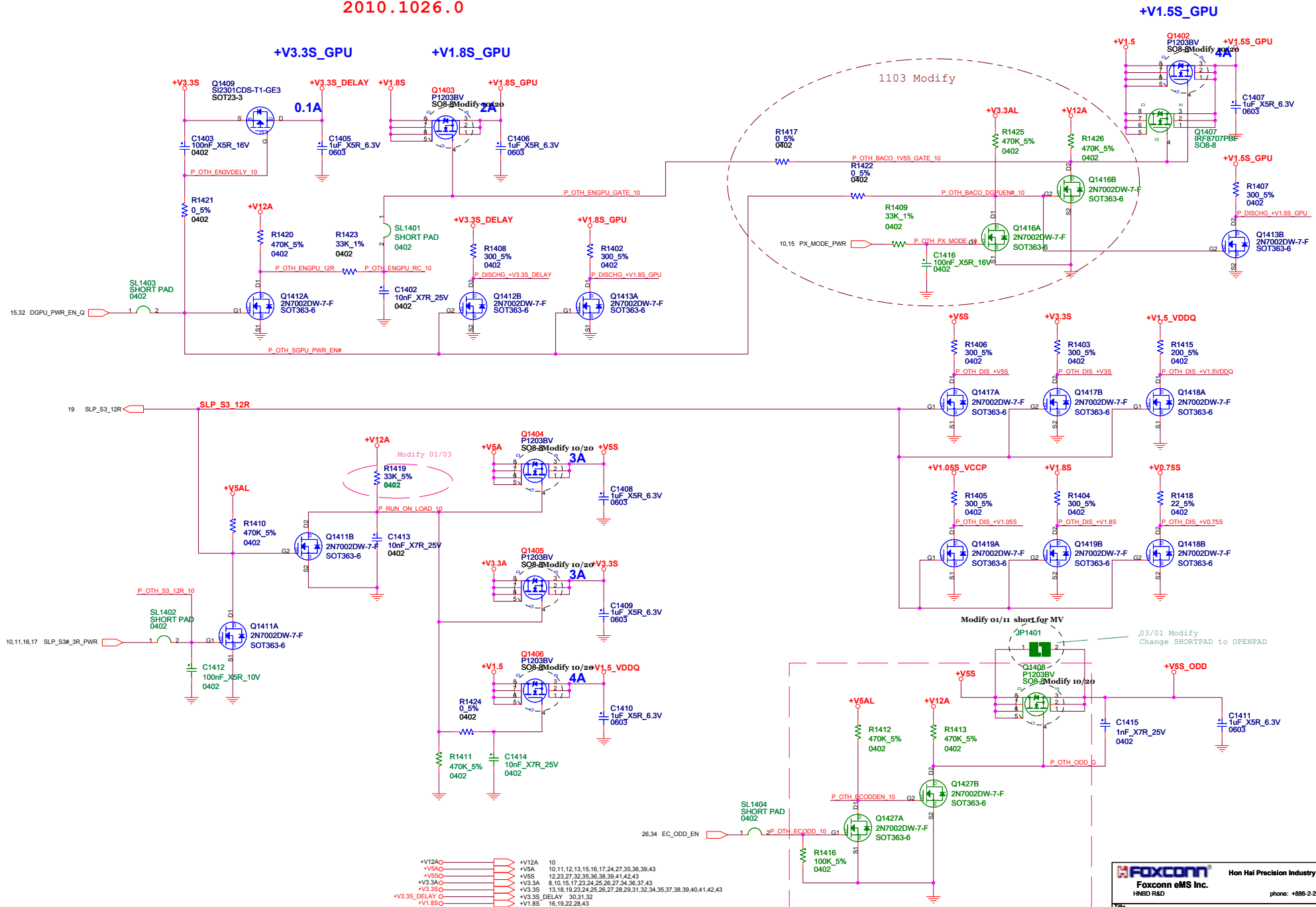


2010.1026.0

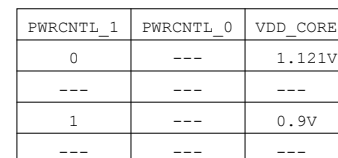


OTHER POWER / DISCHARGE CIRCUITS

2010.1026.0



2010.1026.0



+VBAT		+VBAT	9, 10, 11, 12, 13, 42, 43
+V5A		+V5A	10, 11, 12, 13, 14, 16, 17, 24, 27, 35, 36, 39, 43
+V3_3A		+V3_3A	8, 10, 14, 17, 23, 24, 25, 26, 27, 34, 36, 37, 43
+V3_3S		+V3_3S	13, 14, 18, 19, 23, 24, 25, 26, 27, 28, 29, 31, 32, 34, 35, 37, 38, 39, 40, 41, 42, 43
+V1_SS_GPU		+V1_SS_GPU	14, 30, 32, 33, 43
+VDD_CORE		+VDD_CORE	32, 43
+VPCIE		+VPCIE	30, 31, 32, 43

```
0921 Modify
Port: DGPU_PWR_EN# to DGPU_PWR_EN_Q
Low Active
```

+V1.8S POWER SUPPLY

2010.1025.0

+V1.8S:

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.44A$$

2. Ripple Current:

$$I_{rip} = 0.53A$$

3. Ripple Voltage:

$$ESR/3 = 3.3m\Omega$$

$$V_{rip} = 1.75mV$$

4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 20m\Omega$$

5. MOSFET Spec:

H-side P-MOSFET:

L-side N-MOSFET:

$$R_{ds(ON)} = 110m\Omega \quad (V_{gs} = 4.5V)$$

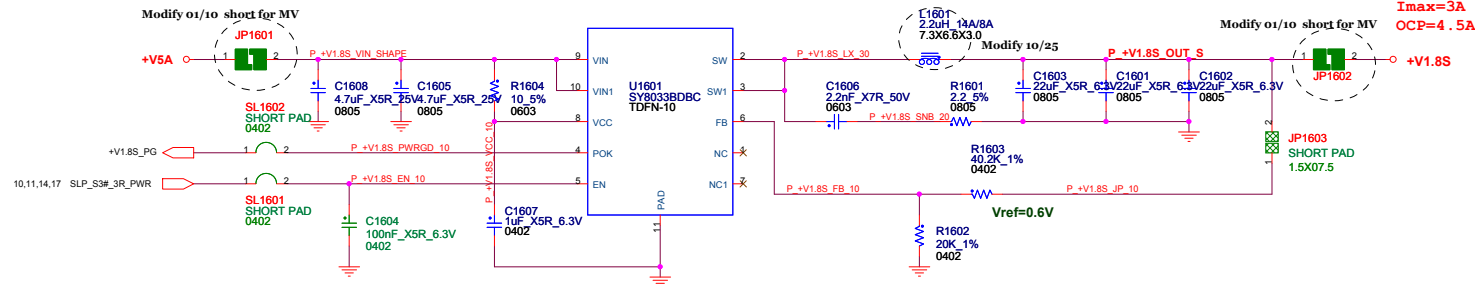
$$R_{ds(ON)} = 75m\Omega \quad (V_{gs} = 4.5V)$$

6. Frequency:

$$F = 1MHz \quad (\min = 800KHz, \max = 1.2MHz)$$

7. OCP:

$$I_{ocp} = 4A(\min) / 4.5A(\text{typ}) / 5A(\max)$$



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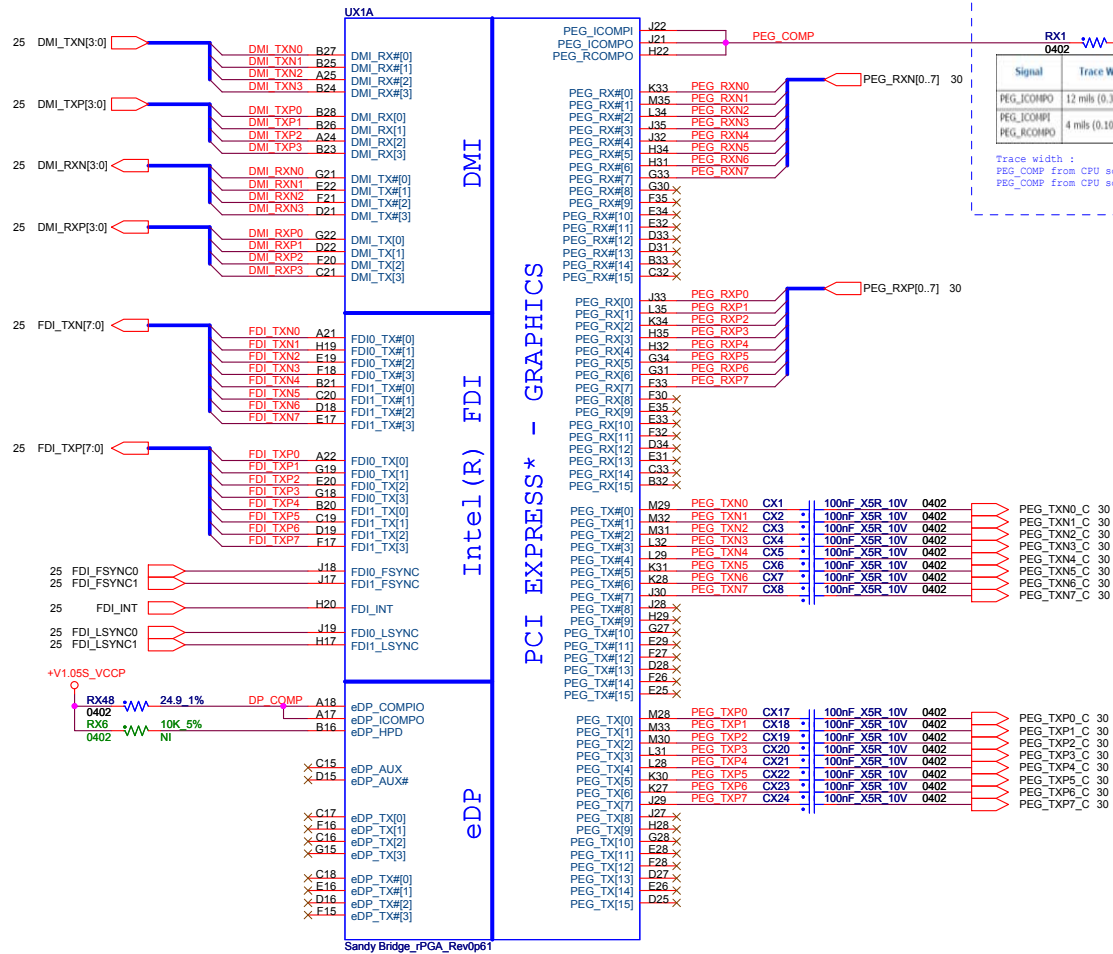
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2010.1026.0



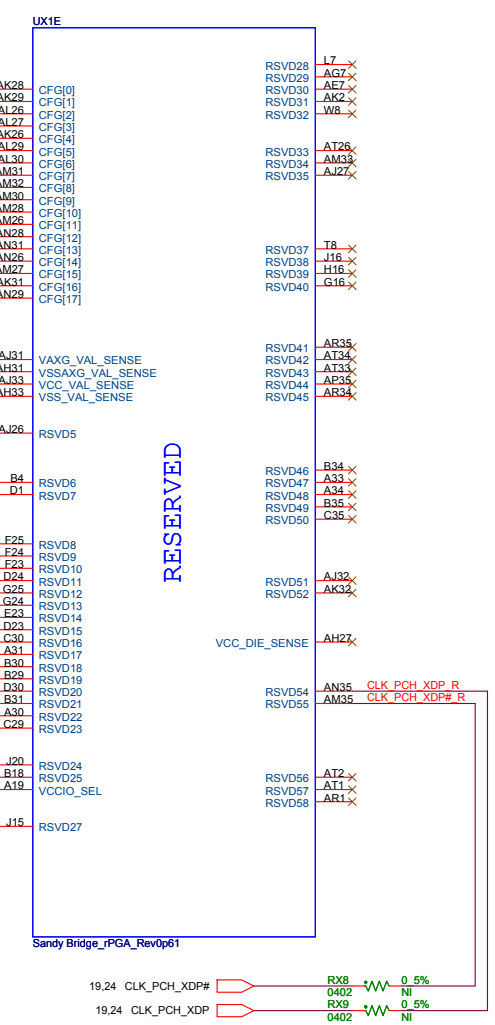
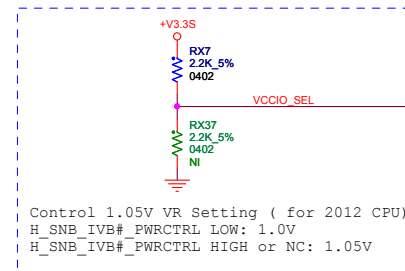
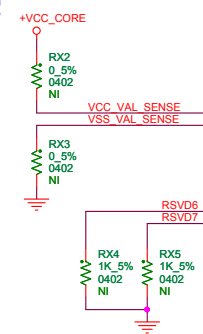
VCCSA_SEL	+VCCSA
H	0.80V
L	0.90V

+V3.3S 13,14,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42,43
+V1.05S_VCCP 11,14,19,21,23,24,25,26,27,28,43



Signal	Trace Width	Trace Spacing to other Signals	Routing Length
PEG_ICOMPO	12 mils (0.305 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)
PEG_ICOMPI	4 mils (0.102 mm)	15 mils (0.381 mm)	500 mils (12.7 mm)

Trace width :
PEG_COMP from CPU socket PIN J22 and J22 to Res RX1 is 4mils
PEG_COMP from CPU socket PIN J21 to Res RX1 is 12mils



Display Port Presence Strap
CFG4 1:(Default) Disabled/No Physical Display Port attached to Embedded Display Port
0:Enabled;An external Display Port is connect to Embedded Display Port

PEG DEFER TRAINING
CFG7 1:(Default) PEG Train immediately following xxRESETB de assertion
0:PEG Wait for BIOS for training

PCIE Port Bifurcation Straps
CFG[6:5] 11:(Default) x16 - Device 1 functions & 2 disabled
10:x8,x8 - Device 1 function 1 enabled ; function 2 disabled
01:Reserved - (Device 1 function 1 disabled ; function 2 enabled
00:x8,x4,x4 - (Device 1 functions 1 & 2 enabled

PEG Static Lane Reversal - CFG2 is for the 16x
CFG2 1:(Default) Normal Operation;Lane # definition matches socket pin map definition
0:Lane Reversed

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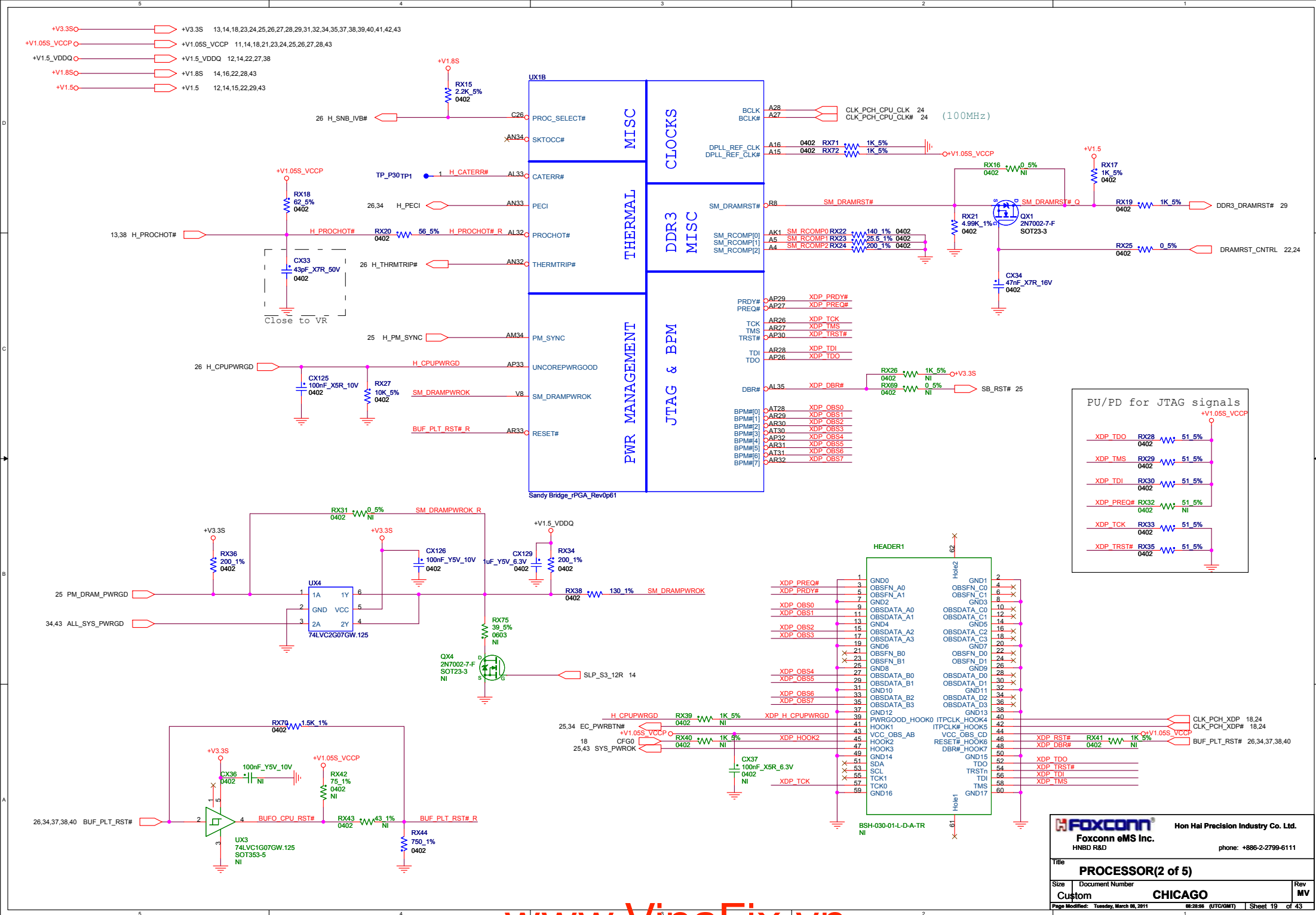
MV

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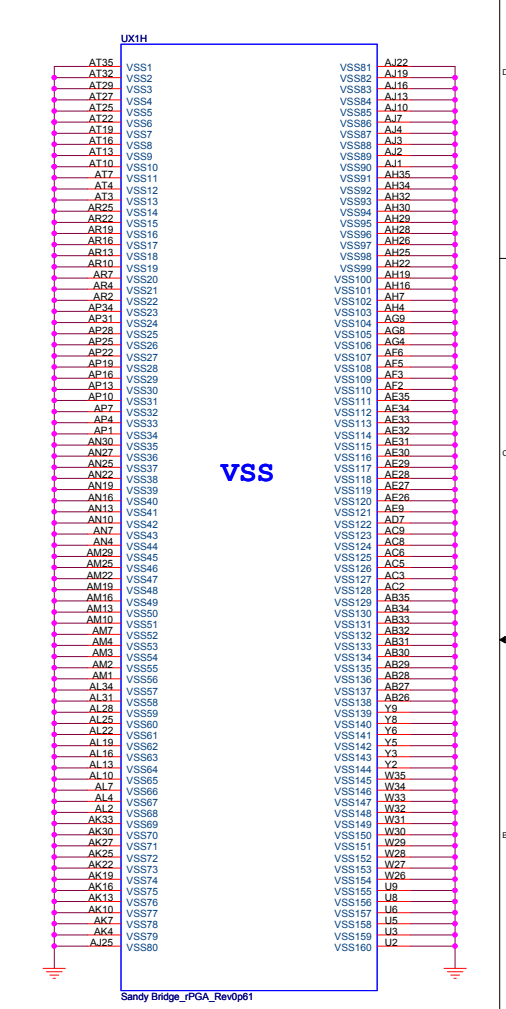
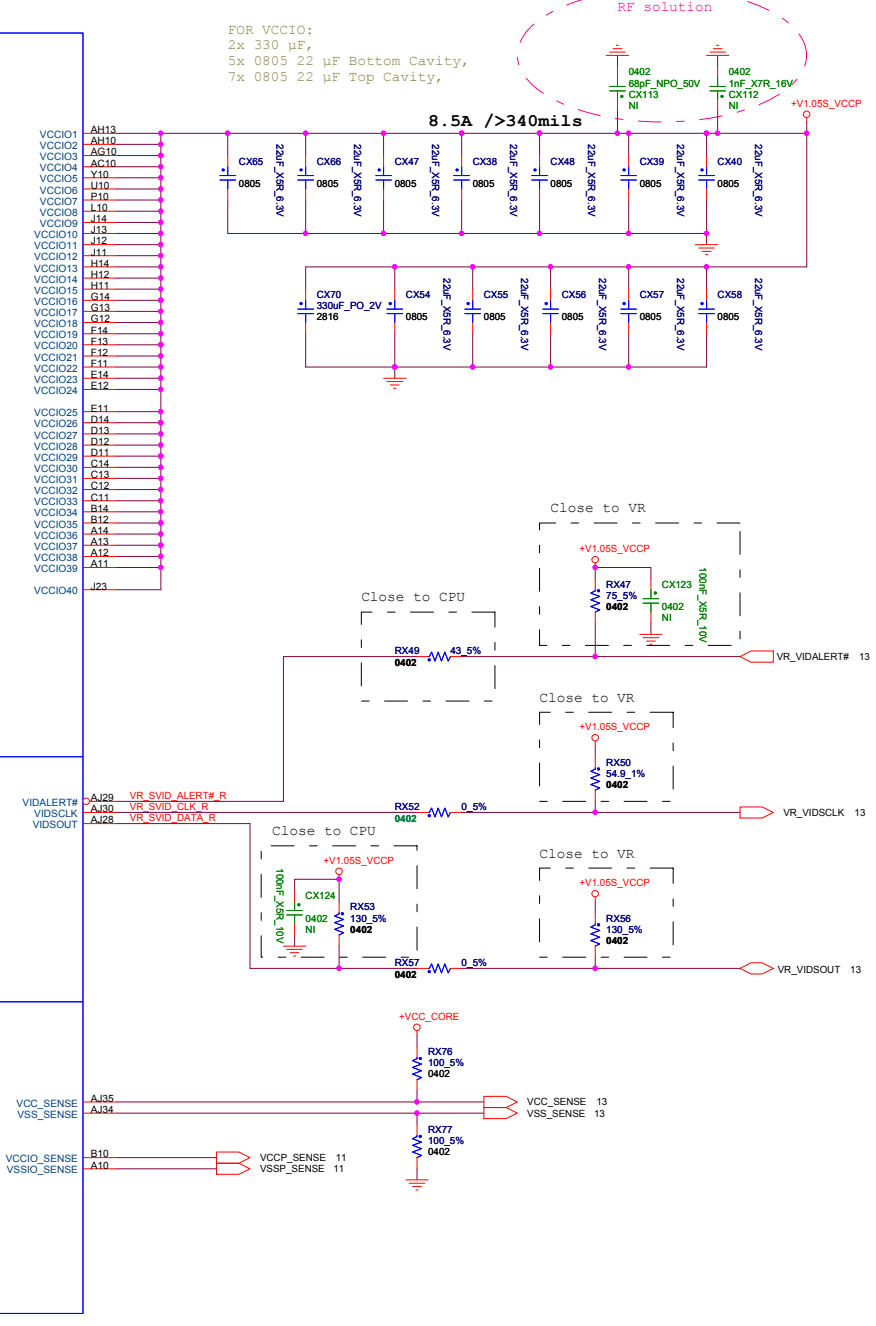
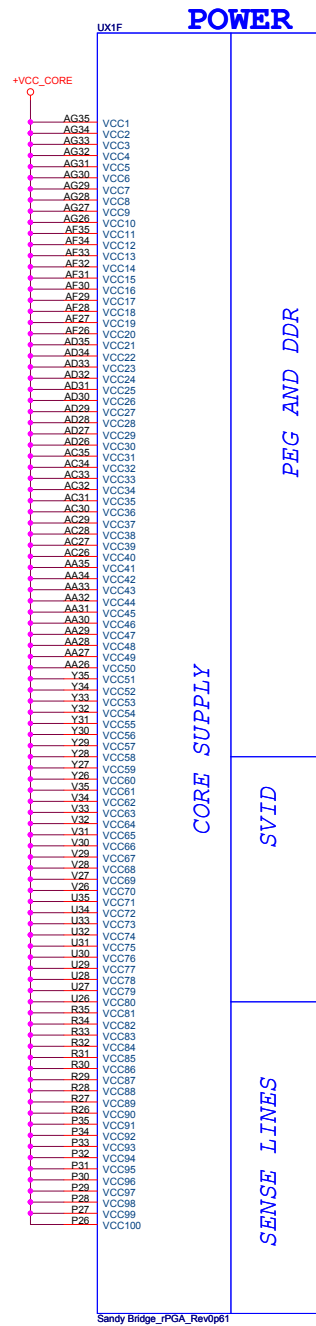
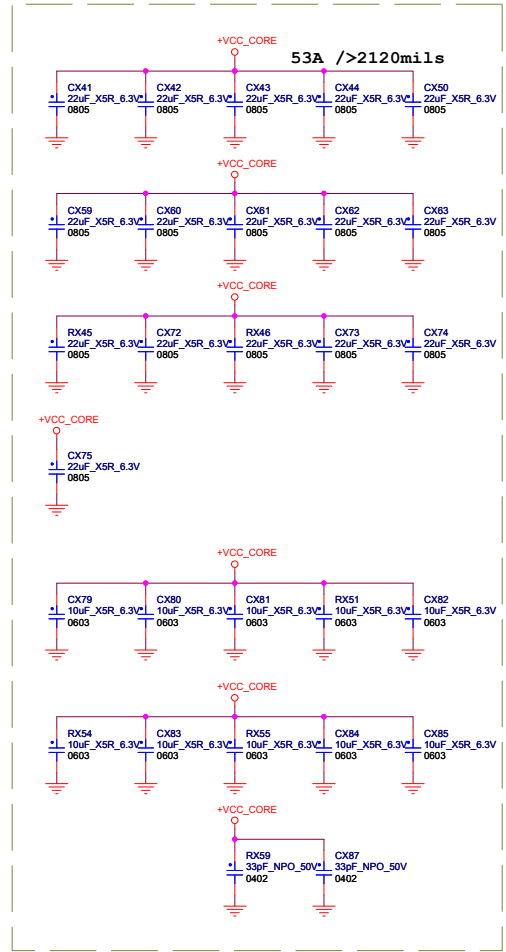
Sheet 18

of 43



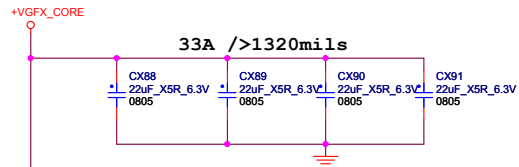
+V1.05S_VCCP 11,14,18,19,23,24,25,26,27,28,43
+VCC_CORE 13,18,43

FOR VCC:
4x 330 μ F Bottom Edge,
10x 0603 10 μ F Bottom Cavity,
8x 0805 22 μ F Top Cavity,
8x 0805 22 μ F Top Edge,

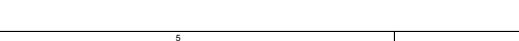
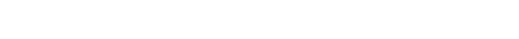
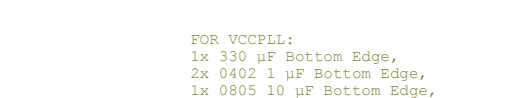
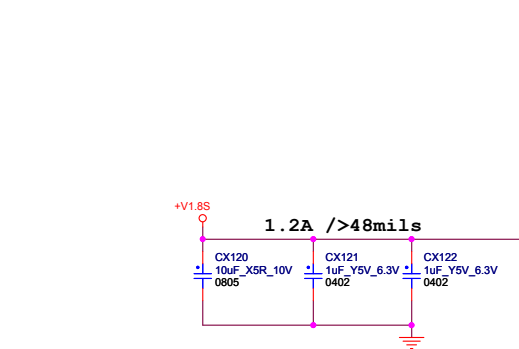
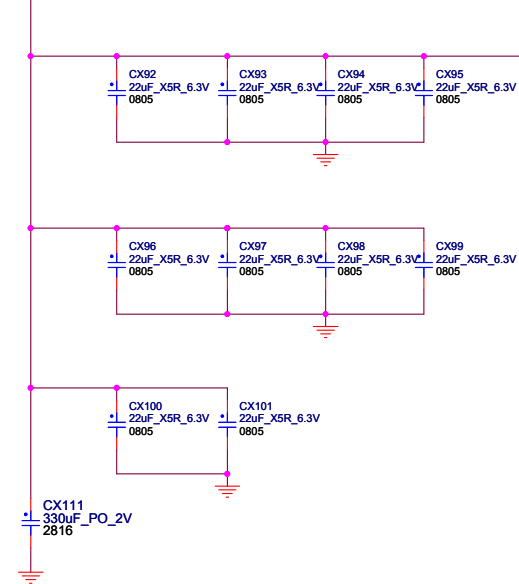


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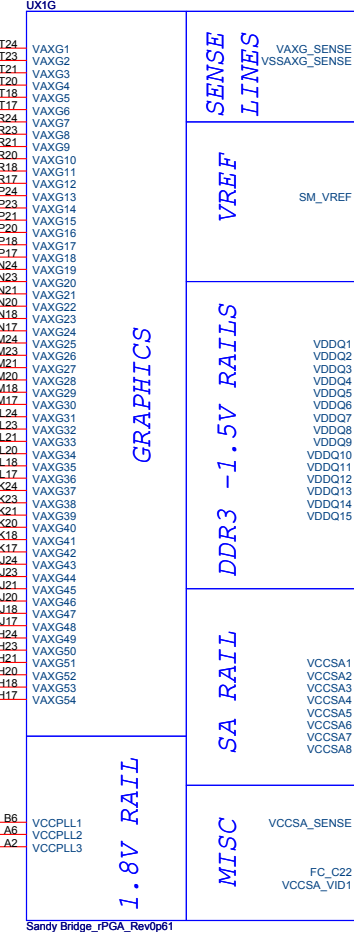
Title		PROCESSOR(4 of 5)	
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Page Modified: Tuesday, March 06, 2011		CHICAGO	MV
08:28:36 (UTC+08:00)		Sheet 21	of 43



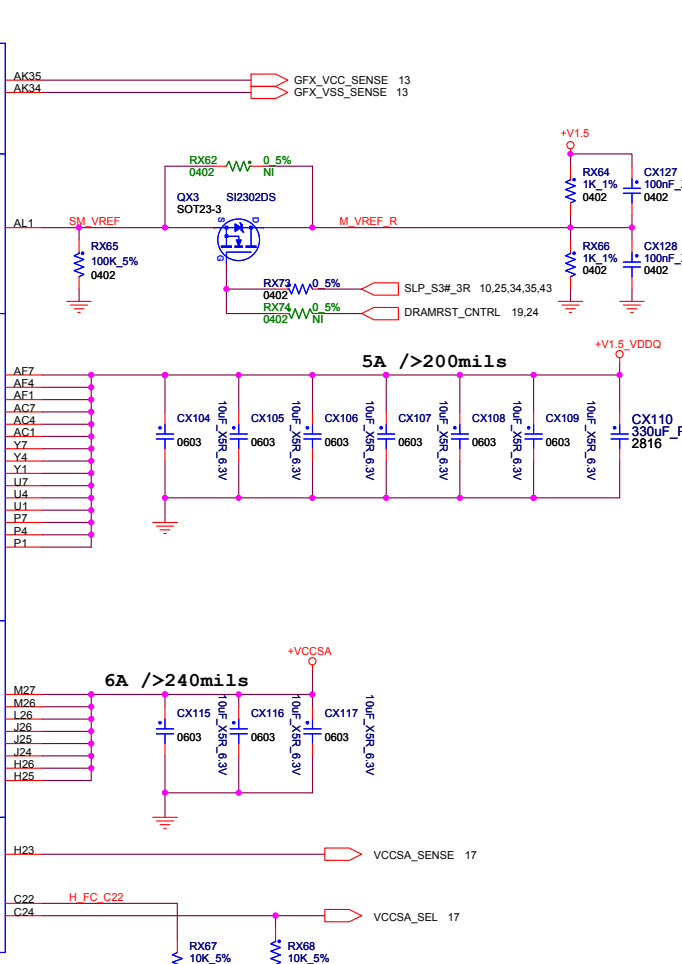
FOR VAXG:
 2x 330 μ F Bottom Edge,
 4x 0805 22 μ F Top & Bottom Cavity,
 8x 0805 22 μ F Top & Bottom Edge,



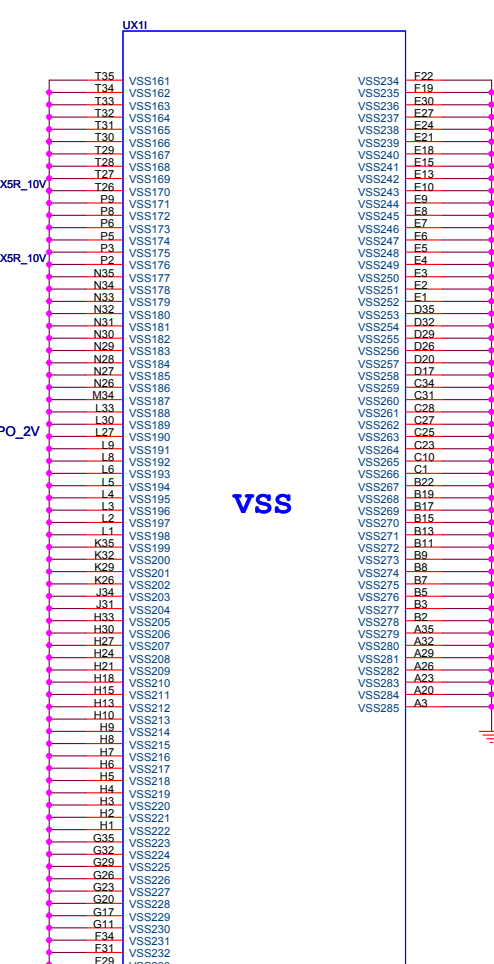
POWER



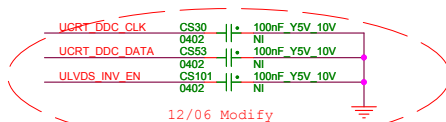
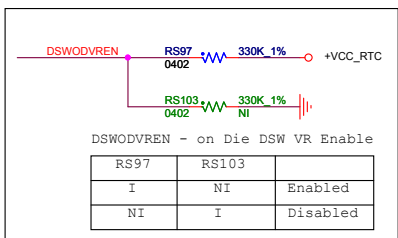
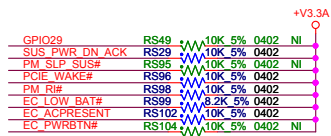
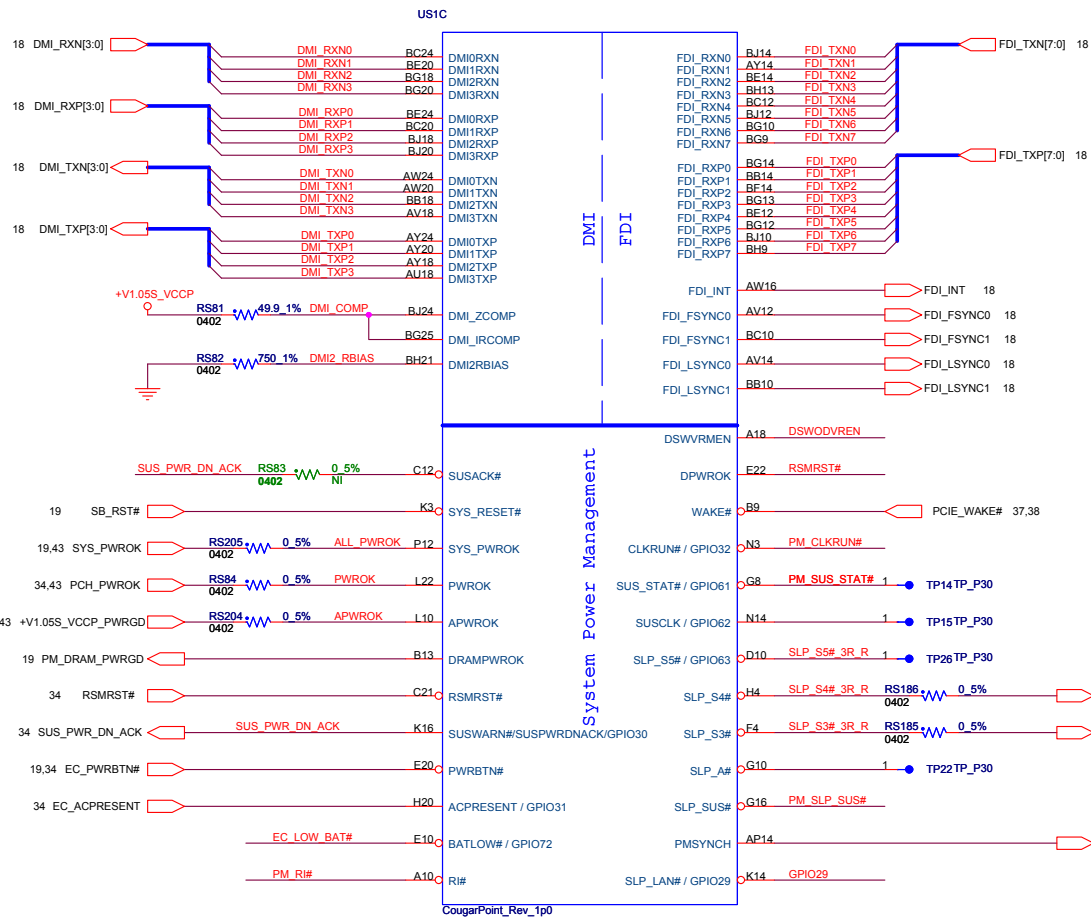
Sandy Bridge_rPGA_Rev0p61



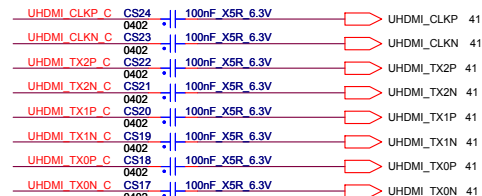
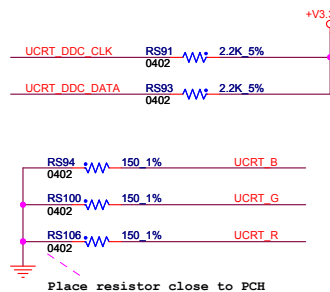
Sandy Bridge_rPGA_Rev0p61



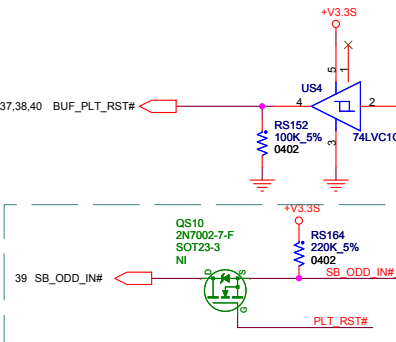
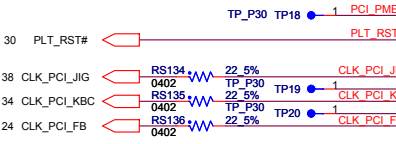
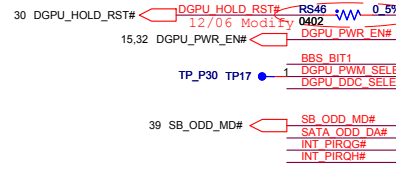
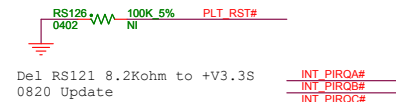
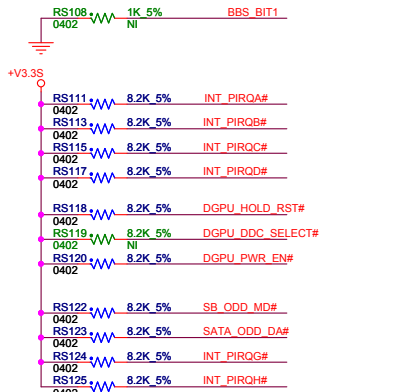
Sandy Bridge_rPGA_Rev0p61



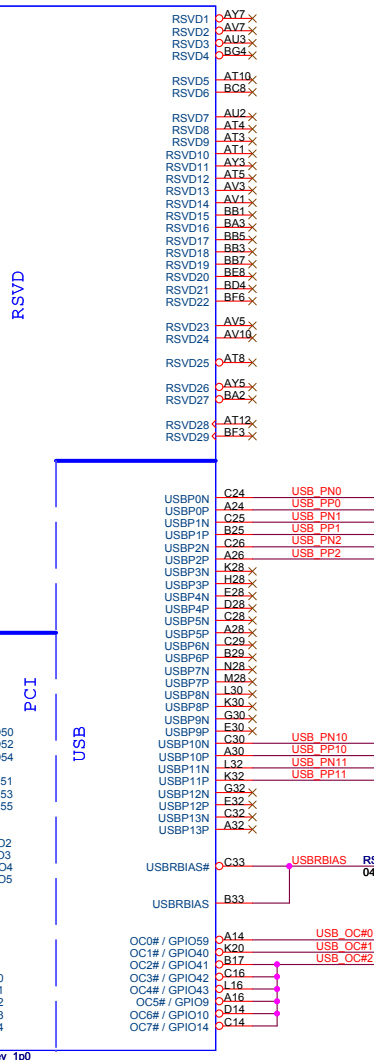
Modify CS30/CS53/CS101 to non-stuff on 01/11



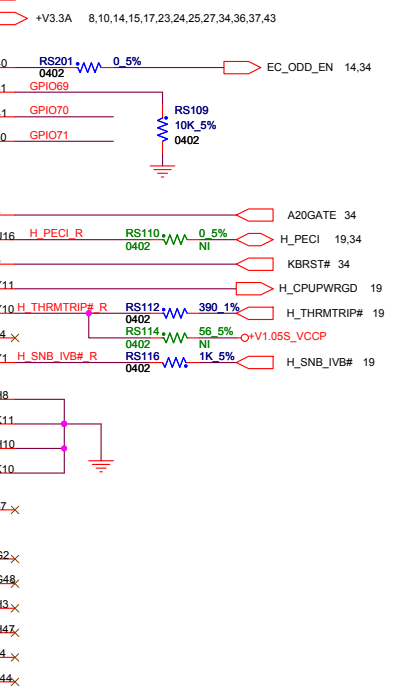
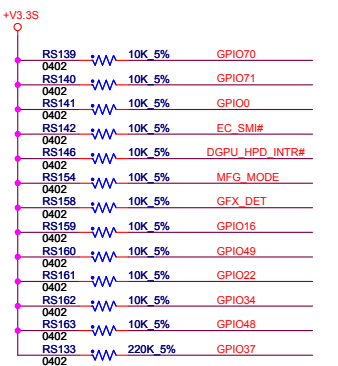
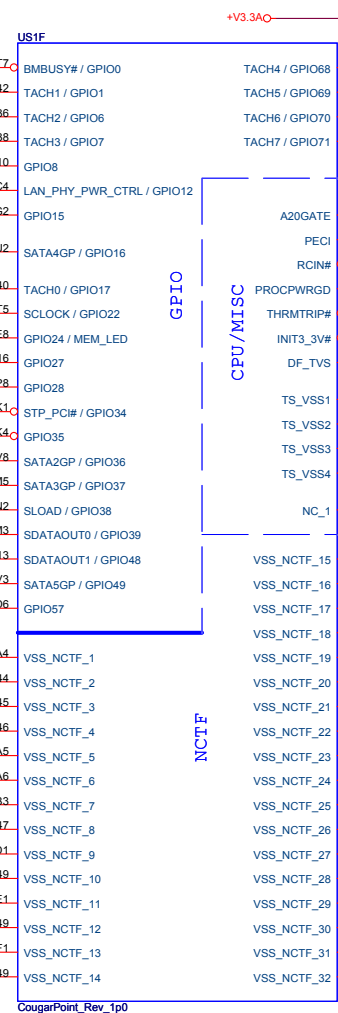
Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



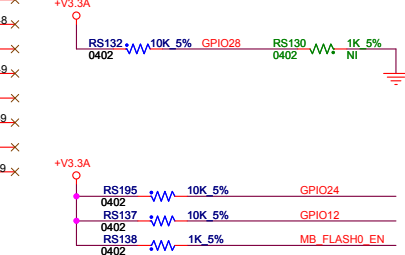
02/24 Modify same as the PV build



USB PORT	Function	OC#
PORT-0	USB Port	OC0#
PORT-1	USB Port	
PORT-2	USB Port	
PORT-3	NC	OC1#
PORT-4	NC	
PORT-5	NC	
PORT-6	NC	
PORT-7	NC	
PORT-8	NC	
PORT-9	NC	
PORT-10	Camera	
PORT-11	WLAN/BT	
PORT-12	NC	
PORT-13	NC	



PLL ON DIE VR ENABLE		
GP28	0	disable
GP28	1	Enable(Default)



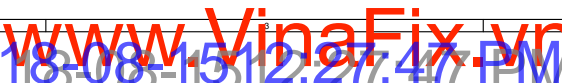
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Title: **CougarPoint(4 of 6)**

Size: Document Number
Custom: **CHICAGO**

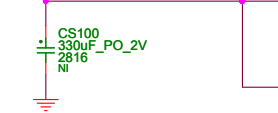
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US11		
AY4	VSS[159]	VSS[259]
AY42	VSS[160]	VSS[260]
AY46	VSS[161]	VSS[261]
AY8	VSS[162]	VSS[262]
B11	VSS[163]	VSS[263]
B15	VSS[164]	VSS[264]
B19	VSS[165]	VSS[265]
B23	VSS[166]	VSS[266]
B27	VSS[167]	VSS[267]
B31	VSS[168]	VSS[268]
B35	VSS[169]	VSS[269]
B39	VSS[170]	VSS[270]
B7	VSS[171]	VSS[271]
F45	VSS[172]	VSS[272]
BB12	VSS[173]	VSS[273]
BB16	VSS[174]	VSS[274]
BB20	VSS[175]	VSS[275]
BB22	VSS[176]	VSS[276]
BB24	VSS[177]	VSS[277]
BB28	VSS[178]	VSS[278]
BB30	VSS[179]	VSS[279]
BB38	VSS[180]	VSS[280]
BB4	VSS[181]	VSS[281]
BB46	VSS[182]	VSS[282]
BC14	VSS[183]	VSS[283]
BC18	VSS[184]	VSS[284]
BC2	VSS[185]	VSS[285]
BC22	VSS[186]	VSS[286]
BC26	VSS[187]	VSS[287]
BC32	VSS[188]	VSS[288]
BC34	VSS[189]	VSS[289]
BC36	VSS[190]	VSS[290]
BC40	VSS[191]	VSS[291]
BC42	VSS[192]	VSS[292]
BC48	VSS[193]	VSS[293]
BD46	VSS[194]	VSS[294]
BD6	VSS[195]	VSS[295]
BE22	VSS[196]	VSS[296]
BE26	VSS[197]	VSS[297]
BE40	VSS[198]	VSS[298]
BE10	VSS[199]	VSS[299]
BE12	VSS[200]	VSS[300]
BE16	VSS[201]	VSS[301]
BE20	VSS[202]	VSS[302]
BE22	VSS[203]	VSS[303]
BE26	VSS[204]	VSS[304]
BE28	VSS[205]	VSS[305]
BE30	VSS[206]	VSS[306]
BE38	VSS[207]	VSS[307]
BE38	VSS[208]	VSS[308]
BE40	VSS[209]	VSS[309]
BE42	VSS[210]	VSS[310]
BF8	VSS[211]	VSS[311]
BG17	VSS[212]	VSS[312]
BG21	VSS[213]	VSS[313]
BG33	VSS[214]	VSS[314]
BG44	VSS[215]	VSS[315]
BG8	VSS[216]	VSS[316]
BH11	VSS[217]	VSS[317]
BH15	VSS[218]	VSS[318]
BH17	VSS[219]	VSS[319]
BH19	VSS[220]	VSS[320]
H10	VSS[221]	VSS[321]
BH27	VSS[222]	VSS[322]
BH31	VSS[223]	VSS[323]
BH33	VSS[224]	VSS[324]
BH39	VSS[225]	VSS[325]
BH43	VSS[226]	VSS[326]
BH7	VSS[227]	VSS[327]
D3	VSS[228]	VSS[328]
D12	VSS[229]	VSS[329]
D16	VSS[230]	VSS[330]
D18	VSS[231]	VSS[331]
D22	VSS[232]	VSS[332]
D24	VSS[233]	VSS[333]
D26	VSS[234]	VSS[334]
D30	VSS[235]	VSS[335]
D32	VSS[236]	VSS[336]
D34	VSS[237]	VSS[337]
D38	VSS[238]	VSS[338]
D42	VSS[239]	VSS[339]
D8	VSS[240]	VSS[340]
E18	VSS[241]	VSS[341]
E26	VSS[242]	VSS[342]
G18	VSS[243]	VSS[343]
G20	VSS[244]	VSS[344]
G26	VSS[245]	VSS[345]
G28	VSS[246]	VSS[346]
G36	VSS[247]	VSS[347]
G48	VSS[248]	VSS[348]
H12	VSS[249]	VSS[349]
H18	VSS[250]	VSS[350]
H22	VSS[251]	VSS[351]
H24	VSS[252]	VSS[352]
H26	VSS[253]	
H30	VSS[254]	
H32	VSS[255]	
H34	VSS[256]	
F3	VSS[257]	
	VSS[258]	

1300mA />52mils



20mA />5mils



2925mA />240mils



50mA />10mils



>10mils



>10mils



POWER

US1G

CRT

VCCADAC

VSSADAC

VCCALVDS

VSSALVDS

VCCTX_LVDS[1]

VCCTX_LVDS[2]

VCCTX_LVDS[3]

VCCTX_LVDS[4]

VCCIO[28]

VCCALLEX

VCCIO[15]

VCCIO[16]

VCCIO[17]

VCCIO[18]

VCCIO[19]

VCCIO[20]

VCCIO[21]

VCCIO[22]

VCCIO[23]

VCCIO[24]

VCCIO[25]

VCCIO[26]

VCC3_3[6]

VCC3_3[7]

VCCVRM[3]

VCCDMI[1]

VCCCLKDMI

VCCDFTM[1]

VCCDFTM[2]

VCCDFTM[3]

VCCDFTM[4]

VCCVRM[2]

VCCAFDIPLL

VCCIO[27]

VCCDMI[2]

VCCSPI

CougarPoint_Rev_1p0

50mA />10 mil



1mA />5 mil



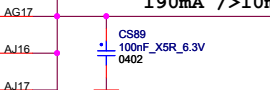
>16mils



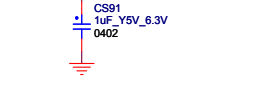
>10mils

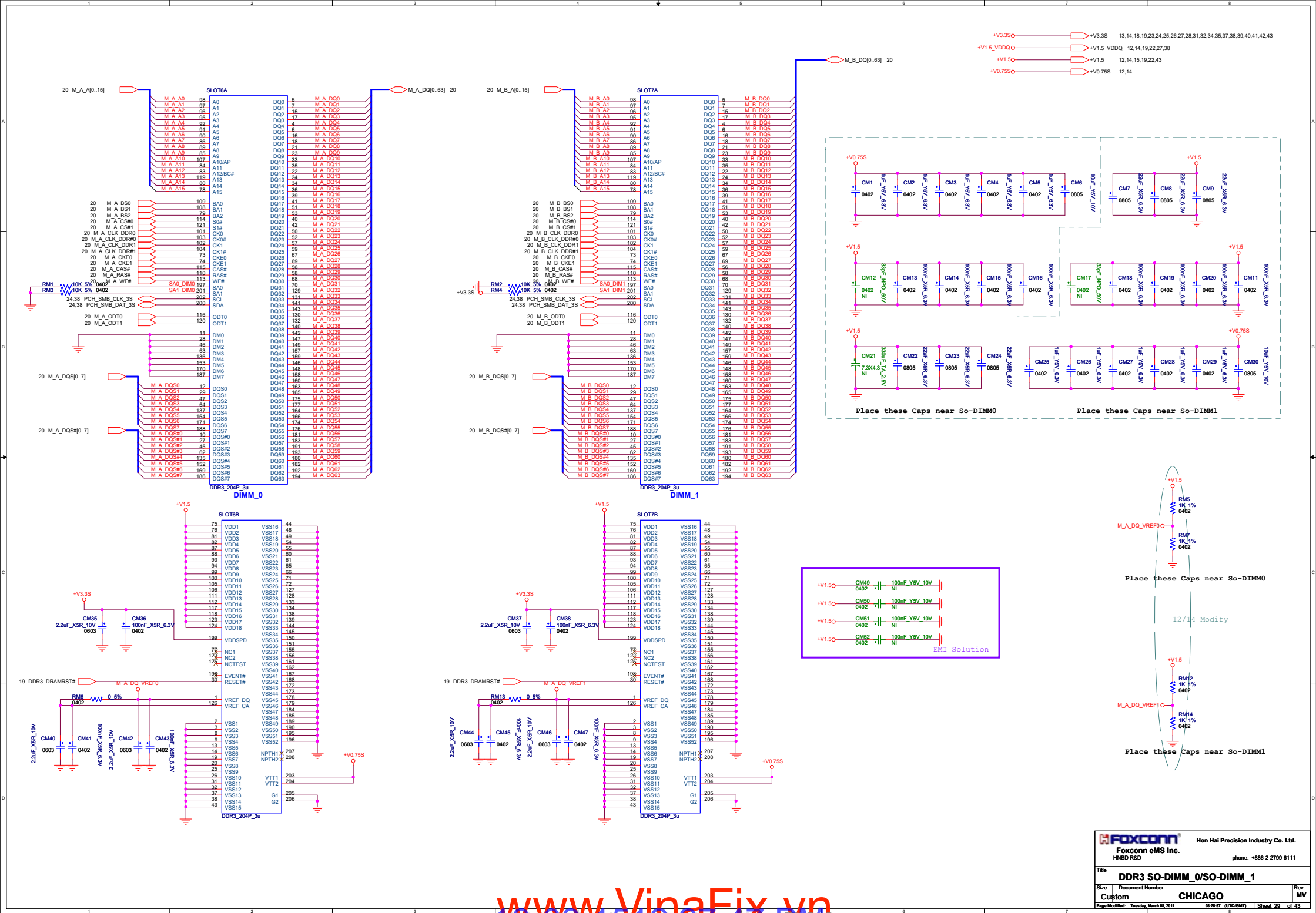


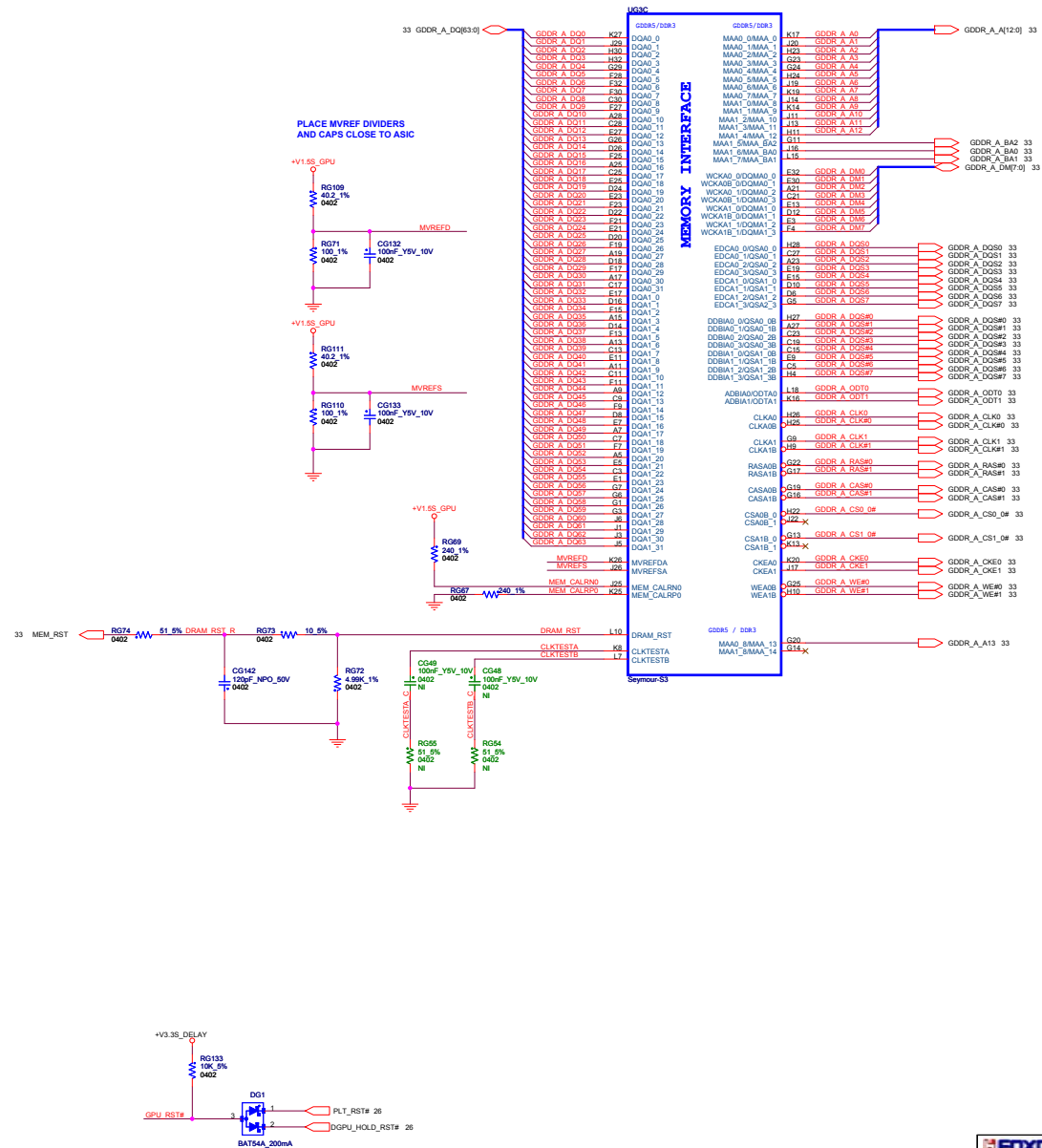
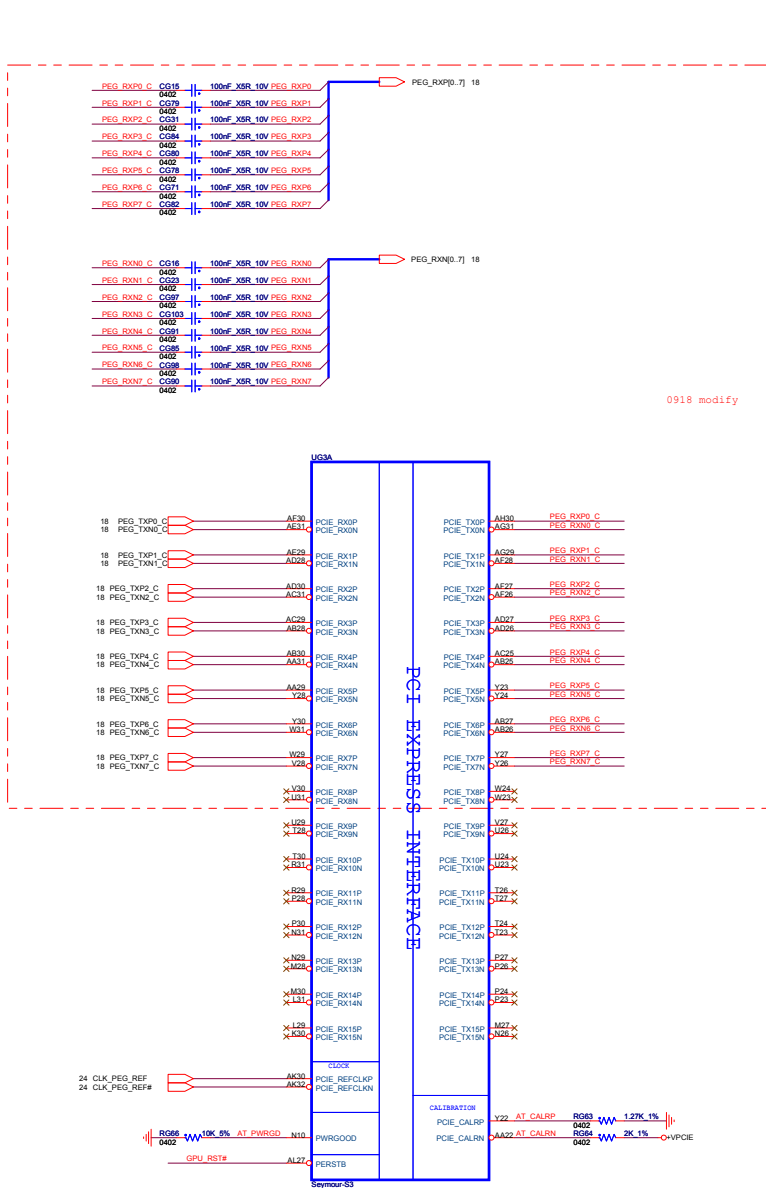
190mA />10mils



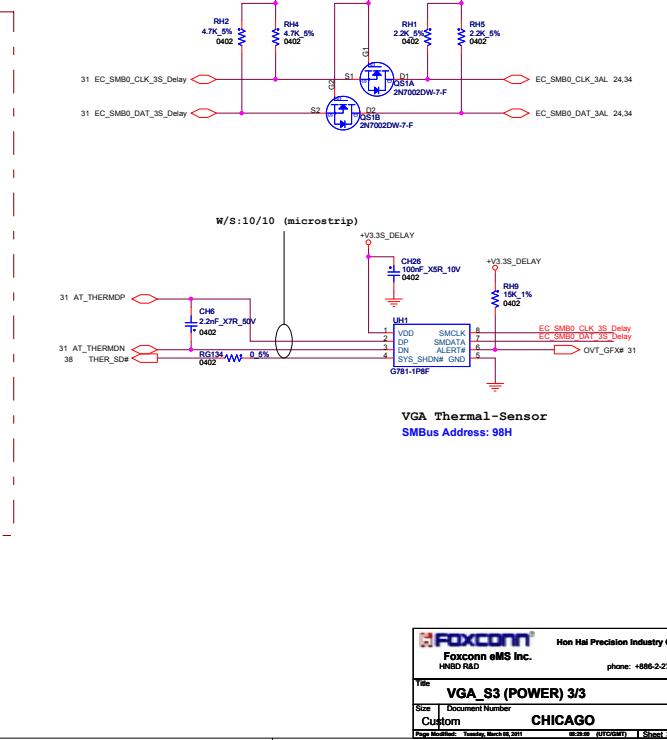
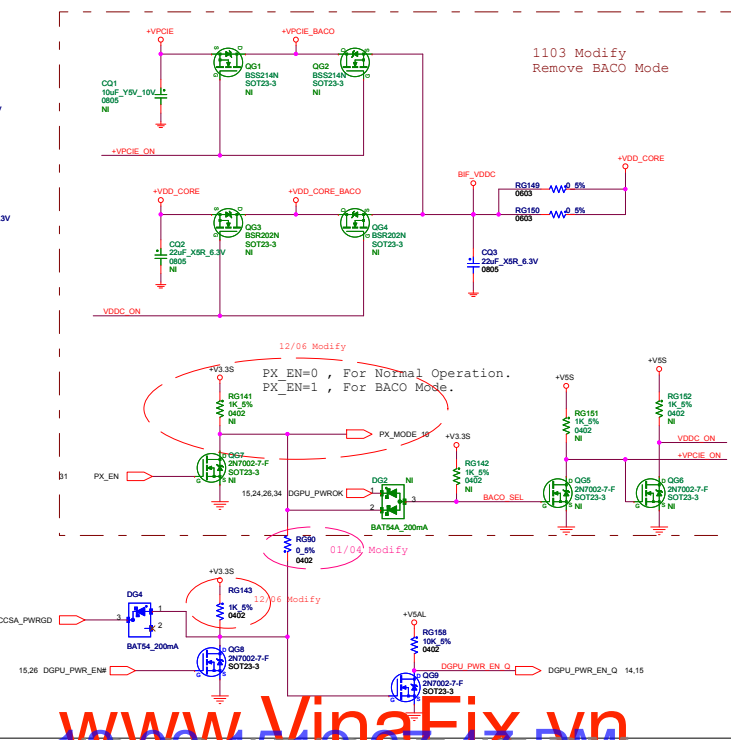
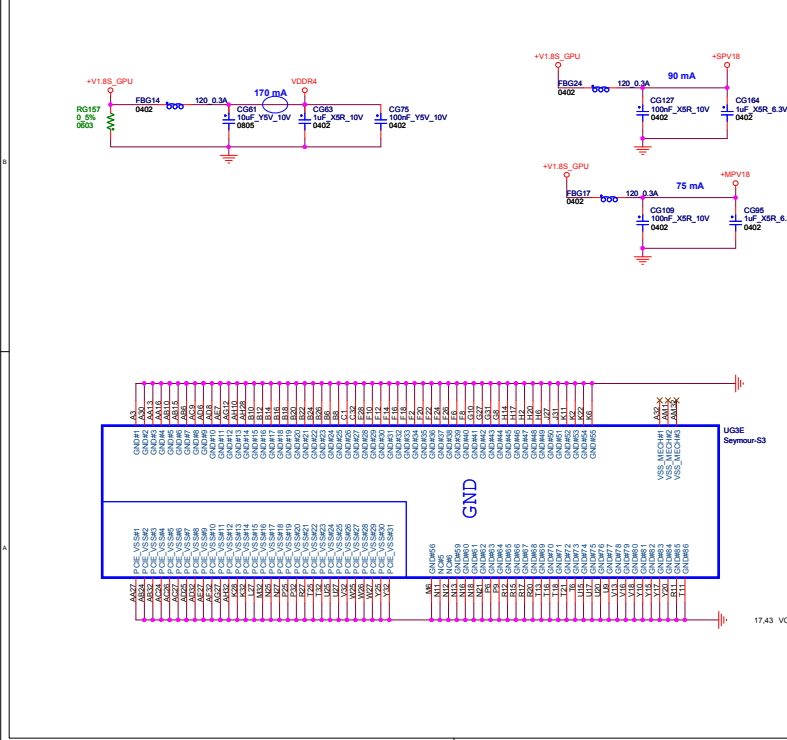
20mA />5mils

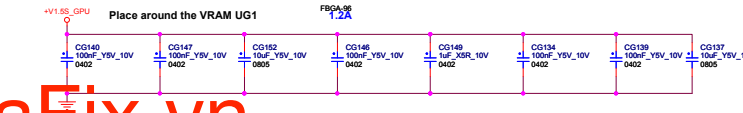
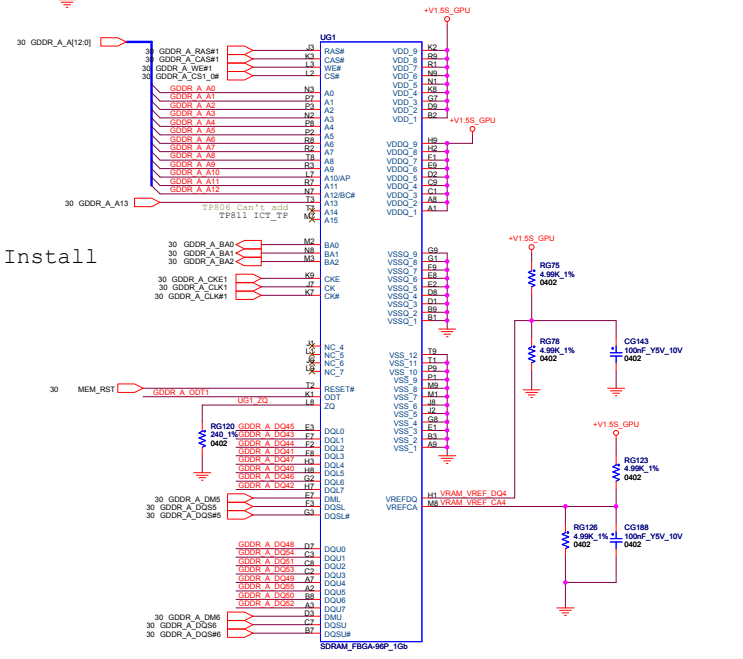
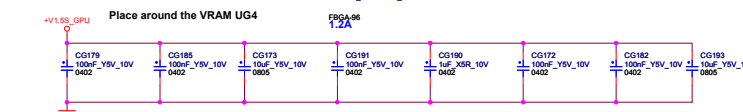
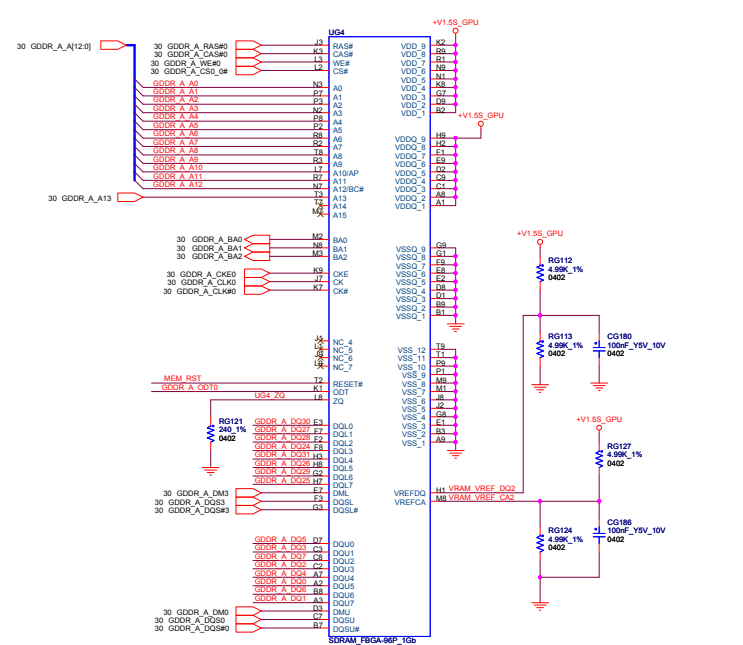




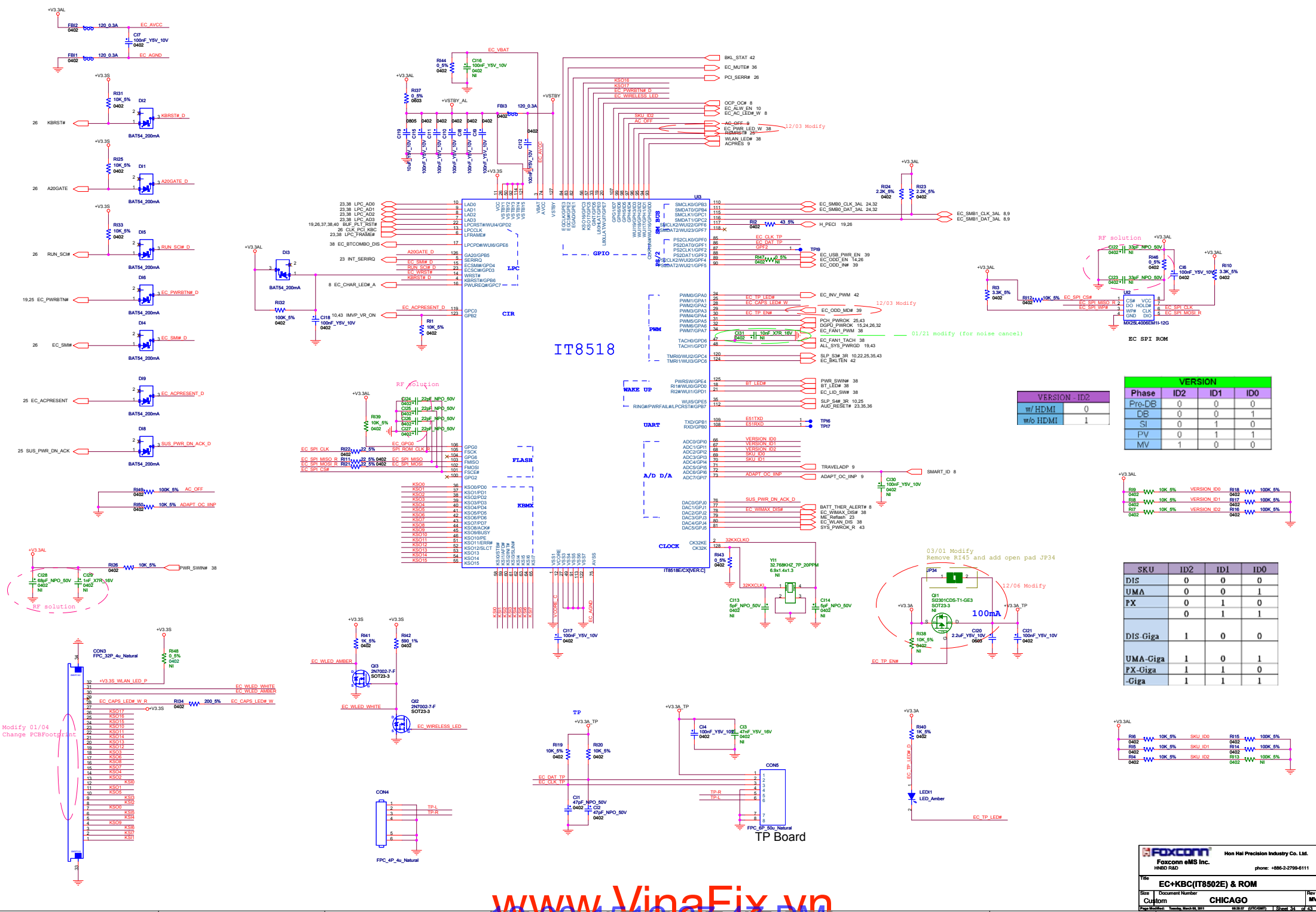








 GDDR_A_DQ[32:63] 30



IT8518

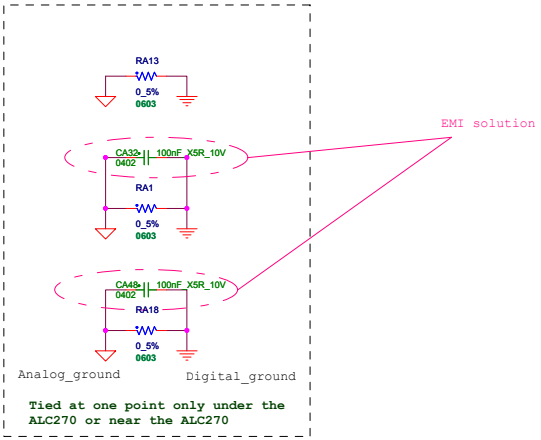
VERSION ID2			
w/HDMI	0		
w/o HDMI	1		

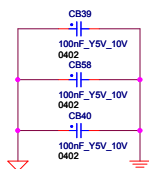
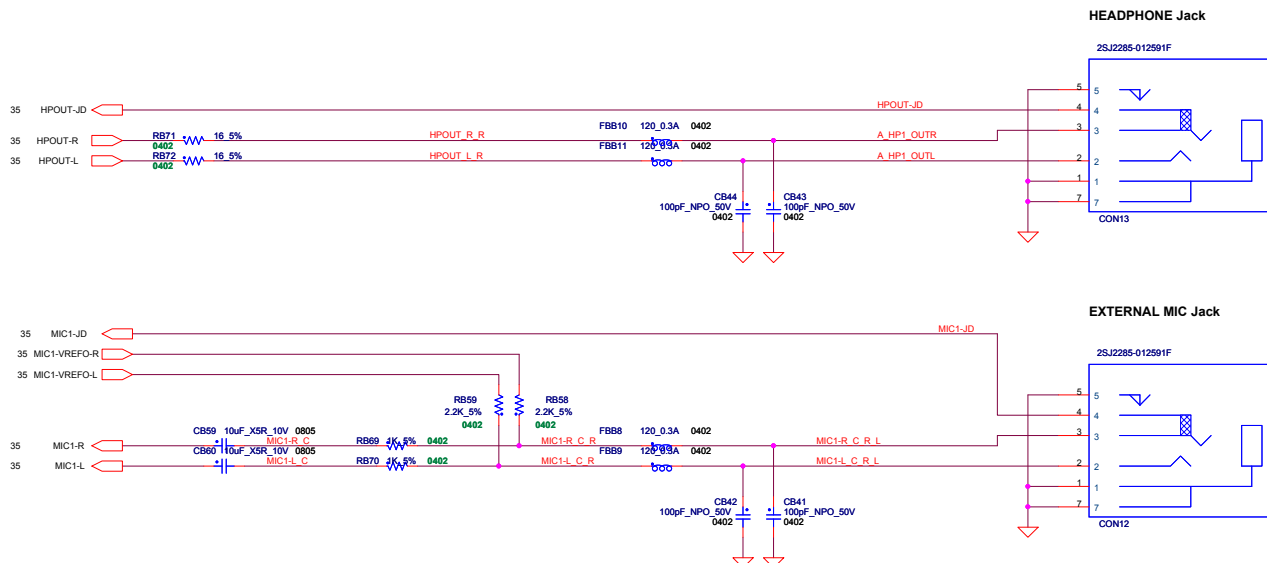
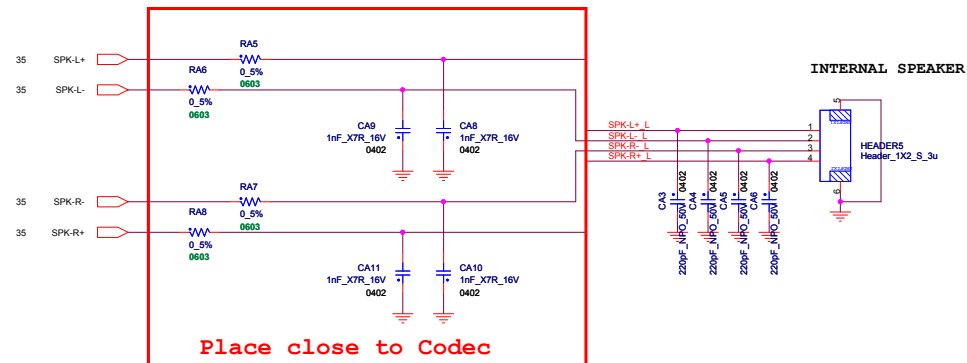
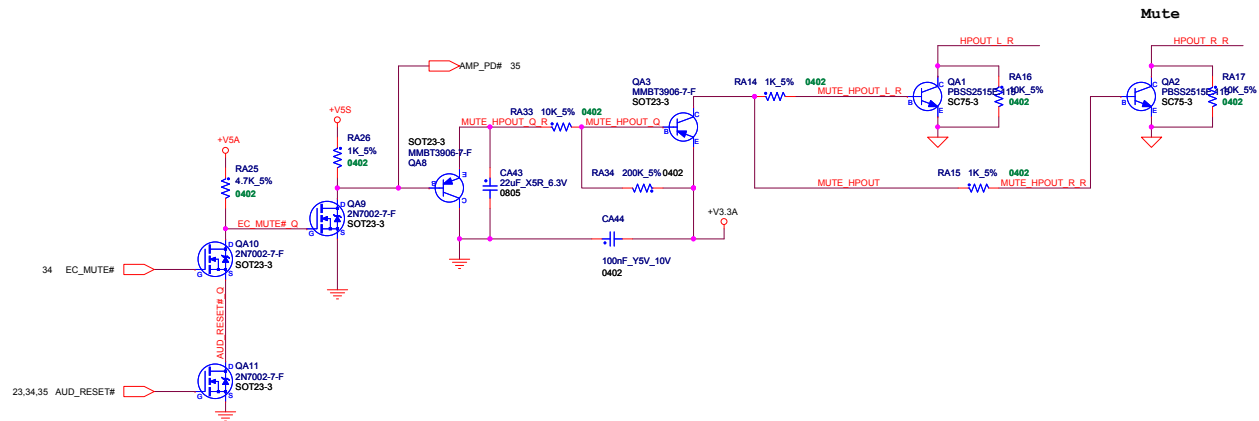
VERSION				
Phase	ID2	ID1	ID0	
Pre-DB	0	0	0	
DB	0	0	1	
SI	0	1	0	
PV	0	1	1	
MV	1	0	0	

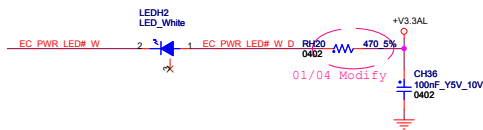
SKU				
ID2	ID1	ID0		
DIS	0	0	0	
UMA	0	0	1	
PX	0	1	0	
	0	1	1	
DIS Giga	1	0	0	
UMA-Giga	1	0	1	
PX-Giga	1	1	0	
-Giga	1	1	1	

<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

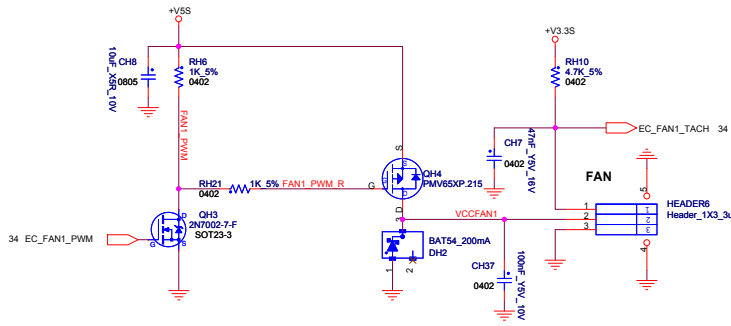
<<Attention>>
For power_On/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before .)





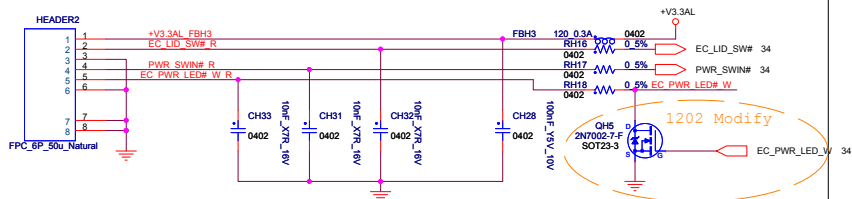


01/04 Modify

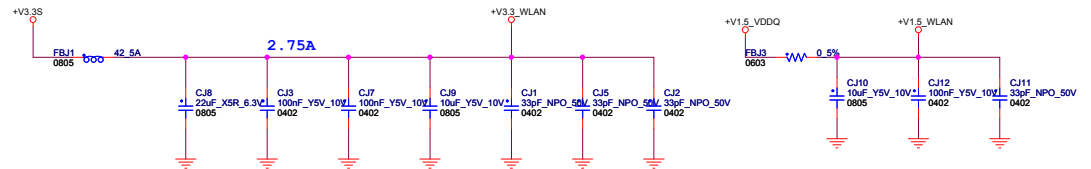


120°C Thermal Shut down
Place Thermal-Sensor near DDR3.

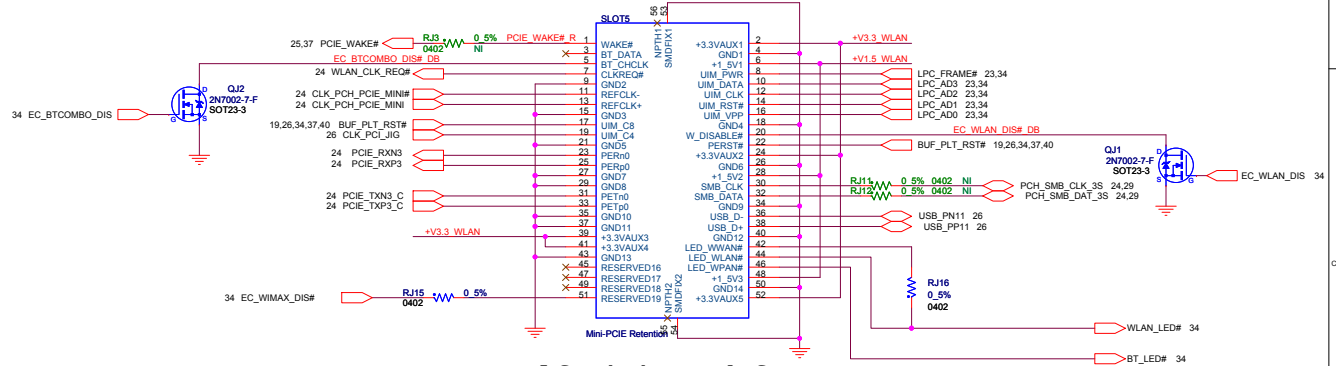
PWR Board CONN.



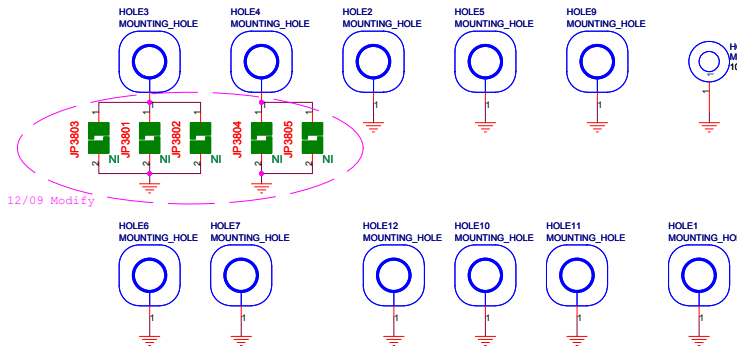
1202 Modify



+1.5V => 0.5A Peak/0.375A Normal
+3.3Vaux => 2.75A Peak/1.1A Normal

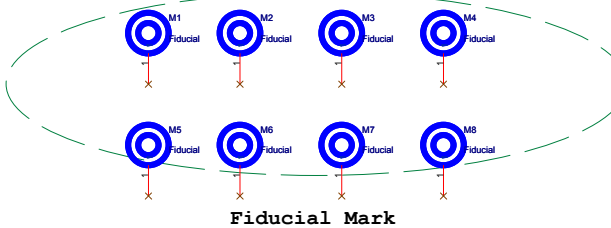


Half Mini Card for WLAN

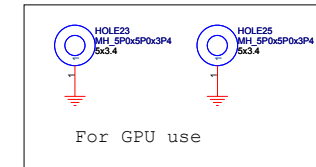


Mounting HOLE

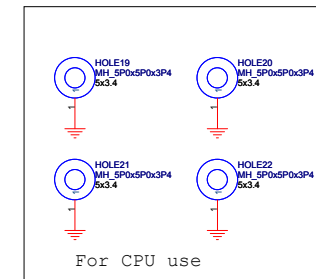
02/09 Modify
Change PCB footprint from FIDUCIAL_IP_3P_B to FIDUCIAL_MARK



Fiducial Mark



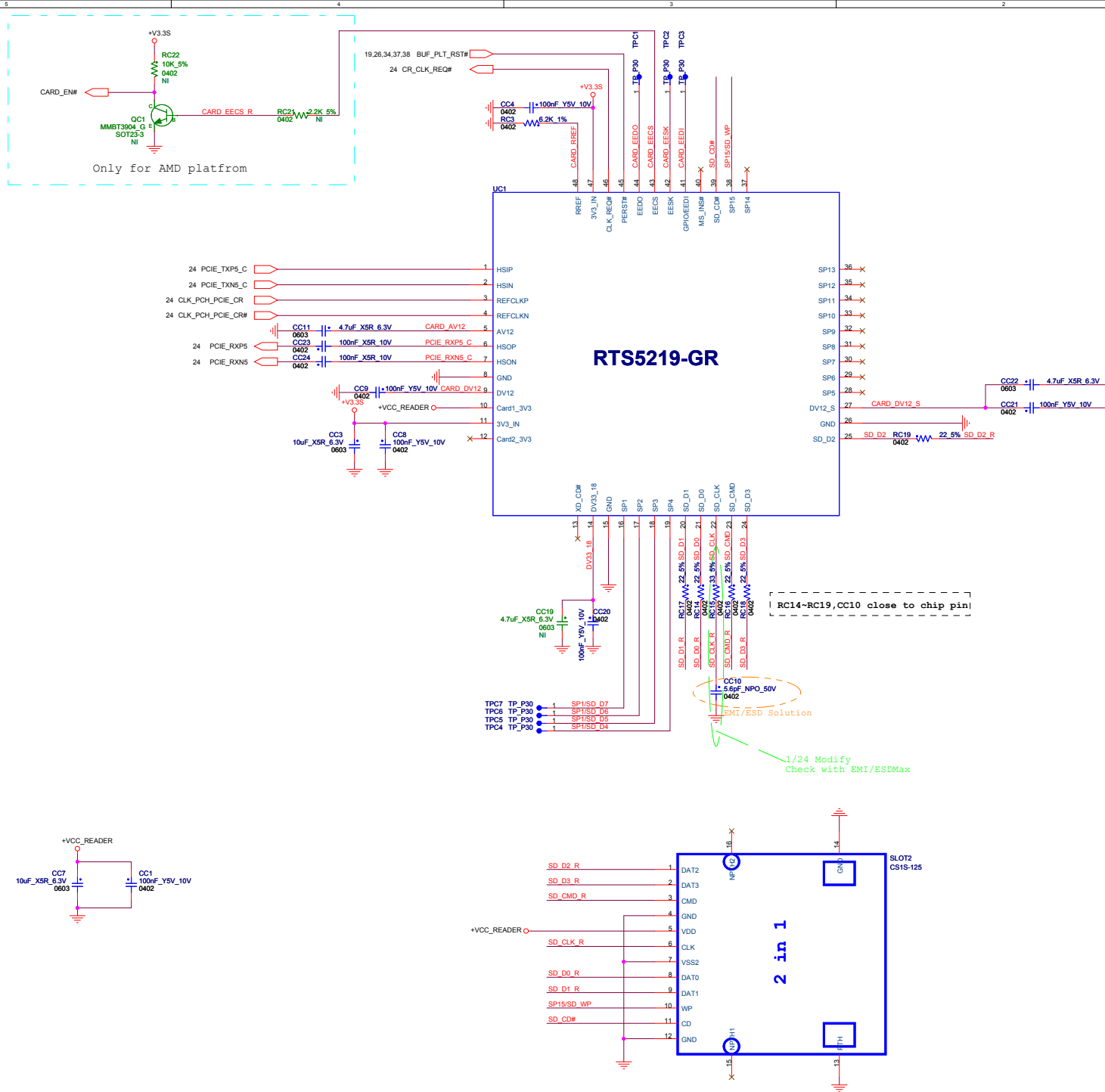
For GPU use



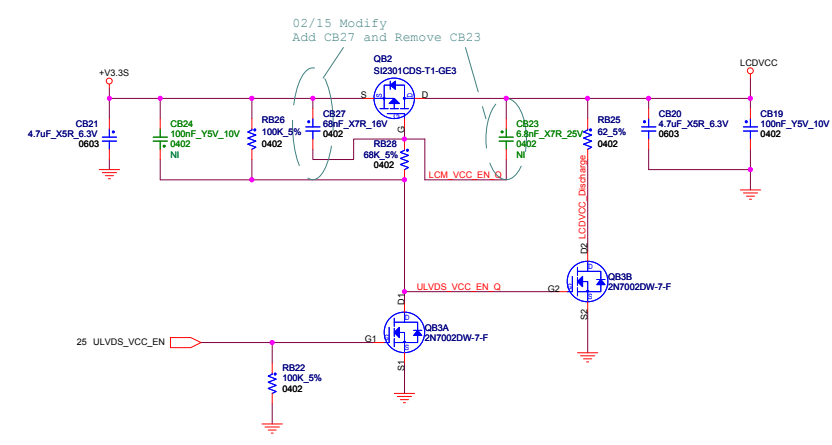
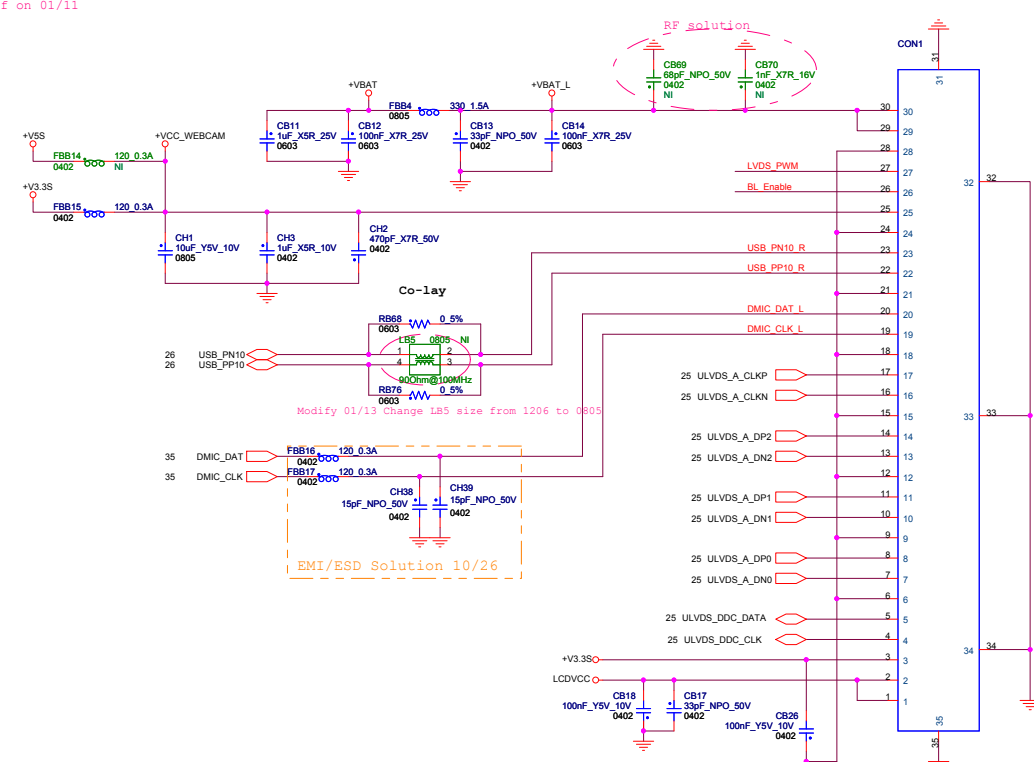
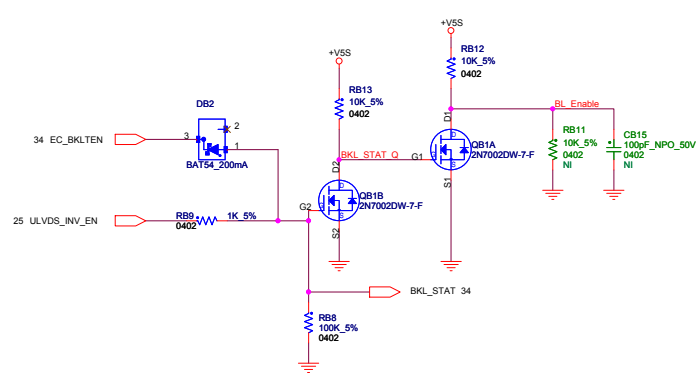
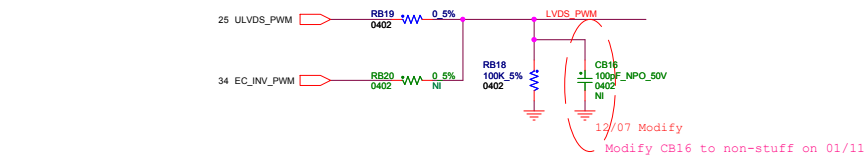
For CPU use

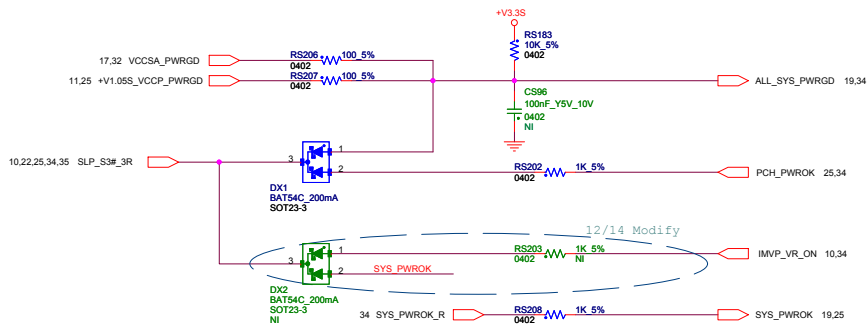
Foxconn Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBQ R&D phone: +886-2-2799-6111	
Title Mini PCIe & RJ11 & BT	Size Document Number
Custom	Rev
Page Modified: Tuesday, March 08, 2011 08:28:00 (UTC+08:00) Sheet 38 of 43	







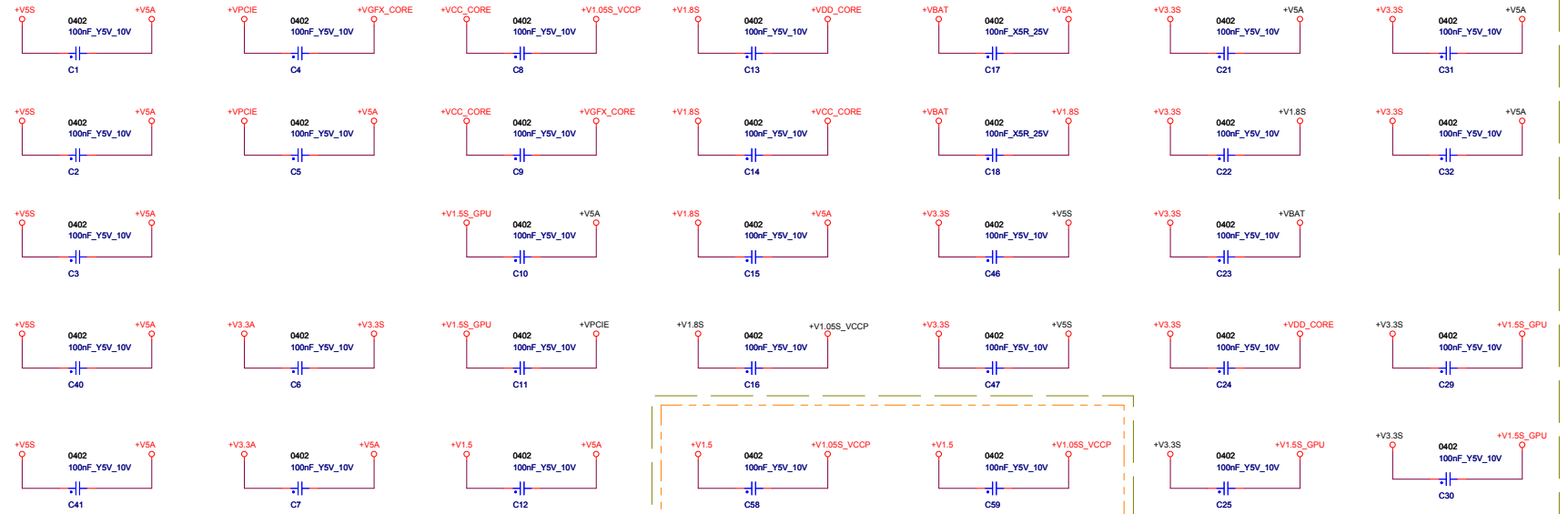
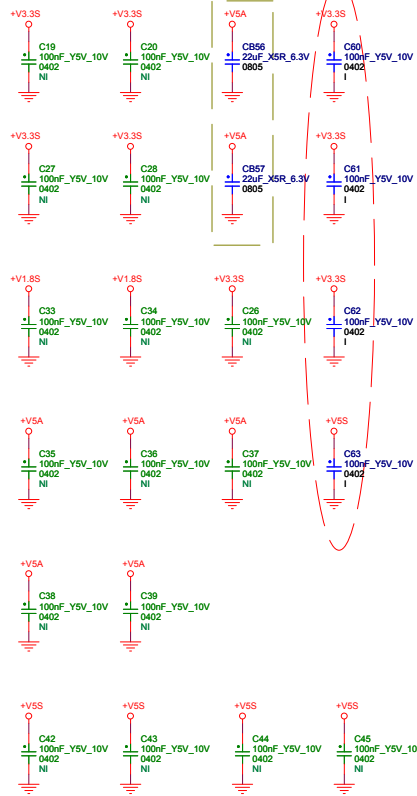




+V5S 12,14,23,27,32,35,36,38,39,41,42
+V3.3S 13,14,18,19,23,24,25,26,27,28,29,31,32,34,35,37,38,39,40,41,42
+V3.3S_DELAY 14,30,31,32

12/07 Modify
1117 Modify

Modify 11/11



EMI/ESD Solution 10/26